Accredited Standards Committee
X3, Information Processing Systems

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Reply to: Lawrence J. Lamers

To: X3T10.1 Membership
From: Lawrence J. Lamers

Subject: Proposed Changes to SSA-PHx for 40 MB/sec

Data Rate

SSA links operate at a peak data rate of 40 MB/s, which is equivalent to 400 Mbits/s on the line.

The minimum overhead imposed by the frame format is 8 characters for a FLAG plus the control, address and CRC fields. If the link is being operated in full-duplex mode there will be an additional overhead of 4 characters for the ACK and RR responses. With 128-byte data fields these overheads lead to the sustained data rates tabulated in table 1~~1~~. The equations used are as follows:

half duplex = 128/(128+8) * 40 MB/sec

full duplex = 128/(128+8+4) * 40 MB/sec * 2 directions

Table 1~~1~~ - Sustained data rate and maximum distance

Nominal speed	Sustained data rate		Maximum distance at full speed
	Half-duplex	Full-duplex	
20 MB/s	18.8 MB/s	2 x 18.3 MB/s	680 M
40 MB/s	37.6 MB/s	2 x 36.6 MB/s	340 M

These data rates assume that there are no transmission errors and that the transmitters and receivers have sufficient buffering to handle back-to-back frames.

The maximum distances allow the responses to be returned within the period of one frame, assuming a propagation velocity of 2×10^8 meters/second. Longer distances are possible at a reduced data rate. However the minimum 25µs ACK time-out imposes an upper limit of 2.5 kilometers. At this distance the maximum sustained data rate would be about 5 MB/s.

The transmit clock shall be accurate to ±250ppm.

The receiver must acquire bit synchronization from the transitions in the transmitted data. If an asynchronous sampling technique is used then the design must take metastability into account.

The receiver shall acquire character synchronization from either of the comma characters, K28.1 or K28.5. Depending on the state of the remote port, one of these characters is sent continuously with alternating disparity when the link is idle. Therefore when the receiver is acquiring synchronization it is sufficient to recognize only one of the 2 possible 10-bit codes for each character. However the receiver must always achieve character synchronization within a total of 200 character periods (100 characters of each disparity.)

Table 22. Driver Output Spectral Content

SPEED	F1	F2	A
200 Mb/sec 400 Mb/sec	80 MHz 160 Mhz	318 MHz 636 Mhz	-11 dBm -11 dBm

Table 433 - Driver System Operating Parameters

SPEED	V1	V2	V3	T1	T3	T5	T8	T10	T11	T12
Mb/sec	mV	mV	mV	ns	ns	ns	ns	ns	ns	ns
200 400	300 300	600 600	1000 1000	0.14 0.07	0.61 0.543 1	2.86 n/a1. 43	3.92 1.491 .96	4.86 2.432 .43	5.00 2.502 .50	5.14 2.592 .57

Table 544. Driver Test Parameters

SPEED	V1	V2	V3	T2	T4	T6	T7	T9	T11	T13
Mb/sec	mV	mV	mV	ns	ns	ns	ns	ns	ns	ns
200 400	300 300	600 600	1000 1000	0.28 0.14	0.75 0.610 .38	3.00 n/a1. 50	3.78 1.421 .84	4.72 2.362 .36	5.00 2.50	5.28 2.64

Table 655. Driver Operating Specifications

Line driver specification:	minimum	nominal	maximum	units
On state output DC current (s)	8.1 mA	9.5 mA	10.9 mA	mA
On state output current imbalance (LineOut+ - LineOut-) (s)	-0.5 mA		+0.5 mA	mA
Off state output DC current (s)	-25 A		+25 A	µA
Output voltage range (s)	1.64 V		4.13 V	V
Output voltage slew rate (ds)			4.0 V/ns	V/ns
Output jitter (peak-peak) * (d)			0.14 ns	ns
Output voltage spectral content (s)	Shall Must be within the envelope (see Figure 8) under the test conditions specified in 7.1.3.4 section			
Output voltage waveform (d)	Shall Must be within pulse mask (see Figure 9) under test conditions specified in 7.1.3 section			
* This is an operating requirement specification. It is the actual jitter allowed under system operating conditions. It is not the result of the tests defined in 7.1.3 specified in section because of the triggering scheme used for these tests. The test conditions in 7.1.3 section result in the observed jitter being twice the value specified in this table. (s) = single ended, (d) = differential				

Table 766. Receiver System Operating Parameters

SPEED	V1	V2	T1	T3	T7	T8	T9	T10
Mb/sec	mV	mV	ns	ns	ns	ns	ns	ns
200	200	1000	0.825	1.825	3.675	4.175	5.000	5.825
400	100	1000	0.413	0.913	1.838	2.090	2.50	2.913

Table 877. Receiver Test Parameters

SPEED	V1	V2	T2	T4	T5	T6	T9	T11
Mb/sec	mV	mV	ns	ns	ns	ns	ns	ns
200	200	1000	1.650	2.650	2.850	3.350	5.000	6.650
400	100	1000	0.825	1.325	1.425	1.675	2.500	3.325

Table 988 - Receiver Operating Specifications

Line receiver specification:	Minimum	Maximum	Units	Notes:
Differential Input Voltage 200 Mb/sec	±200	±1000	mV	Peak Differential. See pulse mask section
Differential Input Voltage 400 Mb/sec	±100	±1000	mV	Peak Differential. See pulse mask section
Input Termination Voltage	2.97	3.63	V	
~~Input Switching Threshold~~	~~0~~	~~±200~~	~~mV~~	~~Hysteresis not required or recommended~~
Common Mode Input Level (peak single ended volts referred to receiver logic ground)		±0.5 DC to 30MHz ±0.1 30 to 500 MHz	V	Caused by common mode noise external to SSA driver
Bit error rate at minimum input pulse mask over required common mode input levels	0	10^{-13}		Test performed according to sections and
~~* The receiver input voltage sensitivity (the minimum differential input voltage that will cause the receiver to detect a logic transition) may be reduced below the 200 mV maximum. The lower this sensitivity voltage the greater the receiver noise margin. Receiver hysteresis is not required or recommended.~~				

Line Segment Termination

Near-end Termination

The following is a modified 7.5 of SSA-PH1 rev 5a.

Specifications For SSA Cable Assemblies

SSA cable assemblies provide the means for connecting SSA ports to each other. The term cable assembly is used in this section because the electrical specifications are between the pins of the connectors and include all the electrical effects of the cable, connectors, backshells, and other hardware necessary to complete the connection. The same specifications apply to link paths provided by backplanes or other means not achieved through the use of extruded, insulated wire. The maximum length of a cable assembly is not specified. However the overall length is a critical parameter in determining if a particular cable assembly will satisfy the SSA specifications.

The position of the cable assembly in an SSA link is shown in n.n and n.n.

The normative requirement for an SSA cable assembly is that it satisfy the required electrical outputs at position M3. (See n.n). Since there are many tradeoffs within a cable assembly that can lead to a satisfactory SSA cable assembly, there are no normative requirements on any of the individual parameters of a cable assembly. Specifically, the conductor material and size, the dielectric material, the shielding method, the line to line skew, and other parameters that describe electrical properties of specific implementations of cable assembly are left as implementor choices.

Since SSA is strictly a point to point technology this specification method applies equally well to individual SSA cable assemblies or to series combinations of assemblies. This means that widely different cable constructions (even within the same SSA link) can be optimized for the specific application.

On the other hand for series combinations of SSA cable assemblies (such as when penetrating a shielded enclosure to form a connection between a shielded external cable assembly and a shielded internal cable assembly) it is necessary that each individual cable assembly be better than the minimum requirements so the series combination will meet the specifications.

An example of a set of electrical parameters that have been found to work well for relatively long copper cables with polypropylene dielectrics is provided for reference in section 0~~0~~.

General requirements for wiring SSA cable assemblies

The signals must “cross over” in all SSA cable assemblies so that outputs are connected to inputs. For example, 'LineOut+' at one port is connected to 'LineIn+' at the other.

The cable shield, or any drain wire that connects to a cable shield within a cable assembly, shall be connected only to the shield of the external connector or to the chassis/ground contact of the internal connector. No shield or drain wire shall be connected to the logic ground connection of the SSA connector on either the driver or the receiver side of the link.

The shield of the bulkhead mounted connector shall be directly connected to the exterior conducting wall of the enclosure that provides the shield function for the enclosure. The effectiveness of this shield connection shall be verified using the test procedures specified in section n.n. Normally 360 degree shielding contacts are recommended.

Equalization circuits may be used on the signal lines within the cable assemblies. These circuits may increase the length of cable that will meet the specifications in this section. All normative specifications apply for both equalized and non-equalized SSA cable assemblies. Note that building equalization into a cable assembly rather than into a receiver will allow a general interoperable system to benefit from the equalization. A general interoperable system is one where any nodes that meet the specifications in section Error! Reference source

not found.~~Error! Reference source not found.~~ may be used. If the equalization is built into the receiver it will not allow longer cables unless ALL SSA nodes used with the longer length also use the same equalization. In effect, using equalization in the receiver integrates the longer cable assembly with that specific node design while putting it in the cable assembly gives the same length benefits to all nodes without the constraining "integration". If equalization circuits are used they shall be placed external to node enclosures.

Test environment for SSA cable assemblies

Refering to n.n, n.n, and n.n the cable assembly test environment uses the same idea for the input (point M2) as for the receiver test and the same idea for the output (point M3) as the driver test. The input signal, M2, is adjusted using a signal degrader to match the minimum pulse mask "eye" for the driver (section n.n) while the output, M3, is measured to determine its relationship to the receiver pulse mask "eye" in section n.n. Cable assemblies whose output does not intrude within the receiver "eye" under these test conditions are acceptable.

The receiver test environment shown in n.n and the associated measurement procedure shall be used to create the input signals at M2. The cable assembly is connected where the receiver is shown in n.n.

It is not required to vary the common mode or ground shift levels for the cable assembly tests.

The driver test load shown in n.n and associated measurement procedure shall be used at point M3 with the scope attached to the cable assembly connector rather than the port connector.

Pulse mask at M2

The input signals for the cable assembly test shall be adjusted for amplitude and jitter to match the weakest allowable driver signal specified in section n.n.

Pulse mask at M3

The output signal for the cable assembly test shall not intrude within the receiver input pulse mask specified in section n.n.

Reference specifications for copper, polymer dielectric, non-equalized SSA cable assemblies

The specifications in Table 9~~Table 99~~ have been found satisfactory for shielded copper, equalized, polymer dielectric SSA cable assemblies of several meters in length.

NOTE: The following table may need adjustment for 400 Mb/sec ljl.

Table 9~~9~~ - Reference specifications for non-equalized copper, polymer dielectric cables

Differential characteristic impedance (Measured with a differential TDR)	150 ohms ±10%
Attenuation (Measured with a network analyzer)	<4.2 dB @ 100 MHz <7.8 dB @ 300 MHz
Skew between conductors in the same signal pair (Measured with a 2 channel TDR)	<1.0 ns
Differential cross talk between signal pairs (near end with 1ns rise time on driven differential pair)	<5%

All measurements are intended to apply to completed cable assemblies. All measurements except possibly cross talk are usually dominated by the cable media and therefore may not require the full cable assembly for execution.

The differential characteristic impedance shall be measured in the following way:

- The length of the cable sample shall be appropriate for the instrumentation.
- The signal pair being measured shall be specified according to its identification and position in the cable layup.

- At the end where the TDR is attached all shields and conductors not directly part of the signal pair under test shall be connected together and grounded.
- All conductors at the far end of the cable shall be left unconnected.

The cross talk shall be measured in the following way:

- The complete cable assembly with connectors and backshells (if used) shall be used.
- A differential voltage signal with a 1 volt peak to peak amplitude and approximately a 1 ns rise/fall time shall be supplied to the near end of the driven pair.
- The driven pair shall be terminated with a 150 ohm resistor at the far end.
- The victim pair (the measured pair) shall be terminated at both ends with a 150 ohm resistor (see Figure 1~~Figure 11~~)

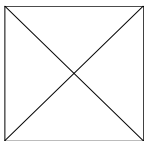

Figure 1~~1~~ - Cable assembly cross talk measurement

The following is a modified 8.2 of SSA-PH1 rev 5a.

Internal port connections

An internal port cable contains 5 conductors. The construction is as specified in 8.5.2.2.

The shield shall be connected to pin 3 in the internal device port bay receptacle which in turn shall be connected to chassis/power ground in the device. Pin 4 in the internal device port bay receptacle shall be logic ground and shall not be connected to the shield in the internal cable assembly. If there is no chassis/power ground available in the device, the shield pin (pin 3) shall be connected to the logic ground on the device side of the connector.

The 5-line connection (section 0~~0~~) uses a balanced shielded cable media. Balanced media require special attention for cable assembly termination so that the logic ground connection remains on the same pin number on both ends is a very minor inconvenience.

Internal device port connector pinouts

The pinout for the signals on the device side of the connector is listed in Table 10~~Table 1010~~. "Device" means disks, controllers or other entities acting as an SSA node.

Table 10~~10~~ - Pinouts for internal port device connectors

Pin	Port device plug & cable receptacle
1	LineOut+
2	LineOut-
3	Chassis/power ground
4	Logic ground
5	LineIn-
6	LineIn+

Internal port 5 line connections

Table 23 defines the pinouts for cable media with 5 lines plus a shield. Note that the shield and the logic ground are connected to the same pin number on both sides in contrast to the lines which are connected to different pin numbers on both sides. This requires careful attention in the cable assembly.

Table 11~~11~~ - Pinout for 5-line internal port device connections

	Receptacle 1		Receptacle 2	
Conductor	Pin	Signal name	Pin	Signal name
1	1	LineOut+	6	LineIn+
2	2	LineOut-	5	LineIn-
Shield	3	Chassis/ power Ground	3	Chassis/ power Ground
3	4	Logic Ground	4	Logic Ground
4	5	LineIn-	2	LineOut-
5	6	LineIn+	1	LineOut+
*Both ends of the shield shall be connected in the cable assembly				