Accredited Standards Committee
X3, Information Processing Systems

Doc: X3T10.1/95A226R1
Date: December 7, 1995
Project: 0989D
Ref Doc.: X3T10.1/
Reply to: Mark DeWilde

To: X3T10.1 Membership
From: Mark DeWilde

Subject: SAT Algorithm Extension for Switches

BACKGROUND

The SAT algorithm as currently defined covers the actions taken by single port nodes which reflect SAT as SAT', and dual port nodes which either may pass SAT, or can be set to reflect SAT as SAT'. There is no permission (or guidance) for a SAT or SAT' character to propagate through a switch, since only reflection is permitted. This proposal would allow port pairs to propagate the tokens to allow cyclic paths containing paired ports to use the same SAT algorithm as loops.

PROPOSAL

Add the following section to TL1 immediately after section 8.5.4 :

8.5.5 Extensions of the SAT algorithm for switches

The extensions to the algorithm for a switch are as follows.

a) Switch ports are paired through the currently defined addressing scheme. Paired ports are treated in the same way as a dual port node, so that both ports are set to transmit SAT and SAT', or both are set to reflect SAT as SAT' and SAT' as SAT.

b) The quotas for port pairs on a switch are set on a pair-by-pair basis. Different pairs of ports on a switch may be set with different quotas to meet the needs of the local sub-web to which they are attached.

c) SAT and SAT' characters are not passed between pairs of ports.

d) SAT timers operate within a pair as they do in single or dual port nodes.

Sincerely,

Mark A. DeWilde
Principal System Architect
Pathlight Technologies

Voice: (607)266-4000 X-403
FAX: (607)266-0352
Email: mark@pathlight.com