Working Draft

T10.1/1146D

Revision 5
March 03, 1997

Information Technology - Serial Storage Architecture - Physical Layer 2 (SSA-PH2)

Preliminary draft proposed American National Standard

This is an internal working document of T10, a Technical Committee of Accredited Standards Committee X3. As such, this is not a completed standard, but is considered to be technically complete by the T10.1 Task Group. The contents of this document may be modified as a result of comments received during the review process.

ABSTRACT

This standard describes the Serial Storage Architecture Physical Layer 2 (SSA-PH2). SSA defines a serial interface hierarchy to be used for purposes within its distance and performance characteristics, including but not limited to storage subsystems.

The Serial Storage Architecture fills a need in the evolution from parallel to serial interfaces for storage devices. It meets the space constraints and cabling considerations for high-density storage arrays with a commensurate improvement in reliability (an architected error recovery, redundant paths to devices, a wrap mode for self-test, line fault detection and a balanced signaling scheme that achieves a low error rate) and configurability (the ability to hot-plug devices, the self-configuration capability, the 20 meter length of cable segments).

The physical layer allows for a CMOS implementation to achieve an economical and small package size, an efficient use of bandwidth, a small frame size to reduce buffer expense and the capability for self-configuration are also needed. The physical requirements include 20 meter distance per cable segment, a small number of signals to limit connector and cable expense, and a low voltage implementation.

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Revision History

Technical changes from rev 4 are shown with revision marks.

T10.1/1146D revision 05 (March 03, 1997)

During the February 25, 1997 T10.1 plenary, I was instructed to generate of revision 5 of SSA-PH2 based off of SSA-PH2 rev 4 with the following modifications:

1) 97a102r3 - Letter ballot comment resolution on SSA-PH2 rev 4.
2) Correct label in Figure 39.

X3T10.1/1146D revision 04 (November 19, 1996)

During the October 30, 1996 X3T10.1 plenary, the generation of revision 4 of SSA-PH2 based off of SSA-PH2 rev 3a with the following modifications:

1) 96a165r1 - Changes to SSA-PH2 rev 3.
2) 96a166r0 - Fiberoptics Annex for TL2 (sic, should be PH2).
3) 96a167r0 - Minutes of SSA-PH2 study group - August 24-26, Boston, MA.
4) 96a169r1 - Changes to SSA-PH2 rev 3a proposal.
5) Figures 2,3,4,5,6,7,10,11,16,40, and 41 were updated (no revision marks).
6) An attempt has been made to only use three fonts: Swis721BT, Monospac821 BT and Symbol.

X3T10.1/1146D revision 03 (August 6, 1996)

During the August 28, 1996 X3T10.1 plenary, I was instructed to generate revision 3 of SSA-PH2 based off of SSA-PH2 rev 2 with the following modifications:

1) 96a142r5 - SSA-PH2 changes proposal.
2) 95a197r1 - Add the HSSDC connector as an alternative external connector. (This new section has not been reviewed as included).

X3T10.1/1146D revision 02 (July 15, 1996)

During the June 26, 1996 X3T10.1 plenary, I was instructed to generate revision 2 of SSA-PH2 based off of SSA-PH2 rev 1 with the following modifications:

1) 96a142r1 - SSA-PH2 changes proposal
2) 96a149r0 - Jitter nulling
3) Style and editorial changes to meet ANSI guidelines.

X3T10.1/1146D revision 01 (May 15, 1996)

During the May 2nd 1996 X3T10.1 plenary, I was instructed to generate revision 01 of SSA-PH2 based off of SSA-PH2 rev 0 with the following modifications:

1) Changes as marked up by the working group.

X3T10.1/1146D revision 00 (April 11, 1996)

During the February 29th 1966 X3T10.1 plenary, I was instructed to generate revision 00 of SSA-PH2 based off of SSA-PH1 rev 9a with the following modifications:

1) Update the boilerplate to SSA-PH2.
2) 95a178r1 - Physical Layer modifications for SSA-40 (Larry Lamers).
3) Expand Figure 19 (Internal unitized backplane connector detail) into two figures to show more detail.
4) Conformance to ANSI standards (96a114r0).

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American National Standard
for Information Systems -

Serial Storage Architecture - Physical Layer 2 (SSA-PH2)

Secretariat
Information Technology Industry Council

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American National Standards Institute, Inc.

Abstract

This standard describes the Serial Storage Architecture Physical Layer 2 (SSA-PH2). SSA defines a serial interface hierarchy to be used for purposes within its distance and performance characteristics, including but not limited to storage subsystems.

The Serial Storage Architecture fills a need in the evolution from parallel to serial interfaces for storage devices. It meets the space constraints and cabling considerations for high-density storage arrays with a commensurate improvement in reliability (an architected error recovery, redundant paths to devices, a wrap mode for self-test, line fault detection and a balanced signaling scheme that achieves a low error rate) and configurability (the ability to hot-plug devices, the self-configuration capability, the 20 meter length of cable segments).

The physical layer allows for a CMOS implementation to achieve an economical and small package size, an efficient use of bandwidth, a small frame size to reduce buffer expense and the capability for self-configuration are also needed. The physical requirements include 20 meter distance per cable segment, a small number of signals to limit connector and cable expense, and a low voltage implementation.

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Foreword (This foreword is not part of American National Standard NCITS.nnn:199x.)

This Serial Storage Architecture - Physical Layer 2 standard is designed to provide a physical layer acceptable to device vendors, looking for an evolution from parallel SCSI, and systems designers looking for opportunities to exploit more fully the capabilities inherent to a serial bus.

This standard was developed by Task Group T10.1 of Accredited Standards Committee NCITS during 1993-96. The standards approval process started in 1995. Annexes A through E are normative, annexes F through K are informative annexes and are not part of the standard.

Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the NCITS Secretariat, Information Technology Industry Council, 1250 Eye Street, NW, Suite 200, Washington, DC 20005-3922.

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Introduction

This standard is divided into the following clauses and annexes.

Clause 1 defines the scope of the Serial Storage Architecture - PH2 (transport layer).

Clause 2 specifies the normative references.

Clause 3 defines the definitions, symbols and abbreviations.

Clause 4 describes the conventions.

Clause 5 defines the modulation scheme.

Clause 6 defines the port data rate.

Clause 7 defines the electrical requirements.

Clause 8 defines the interconnection requirements.

Annexes A, B, C, D and E are normative.

Annexes F, G, H, I J and K are informative.

American National Standard
for Information Systems -

Information Technology - Serial Storage Architecture Physical Layer 2 (SSA-PH2)

1 Scope

The SSA-PH2 standard defines a physical layer that support the SSA transport layer 2 (see SSA-TL2) and any protocols supported by SSA-TL2.

The goals of SSA-PH2 are:

a) extend the cable distance;
b) copper cable operation at 40 MB/s;
c) full duplex operation to achieve an aggregate 80 MB/s between two ports;
d) and other capabilities that fit within the scope of SSA-PH2 that may be proposed during the development phase by the participants in the project.

This document defines the physical layer 2 (SSA-PH2) of the Serial Storage Architecture (SSA). SSA defines a serial interface hierarchy to be used for purposes within its distance and performance characteristics, including but not limited to storage subsystems. This standard is intended to be used with an upper layer protocol [e.g., SCSI-2 Protocol (SSA-S2P) or SCSI-3 Protocol (SSA-S3P)] and a transport layer [e.g., SSA Transport Layer 2 (SSA-TL2)].

A major goal of the SSA-PH2 standard is to define a physical layer acceptable to device vendors, looking for an evolution from parallel SCSI or SSA-PH1, and systems designers looking for opportunities to more fully exploit the capabilities inherent to a serial bus.

1.1 SSA-PH2 characteristics

This standard defines the physical medium (e.g. encoding, modulation, clocking, line drivers/receivers, connectors and cables).

The essential characteristics of SSA-PH2 include:

a) links using copper cable assemblies have been demonstrated to operate at 40 MB/s up to 20 m with on-chip CMOS drivers;
b) support for optical transducers that allow longer distance connections;
c) the link makes optimum use of the physical medium by using full-duplex communication to avoid arbitration overhead and turn-around delay;
d) full duplex communication achieves an aggregate 80 MB/s bandwidth (40 MB/s in each direction) between two ports;
e) the cables and connectors are physically compatible with small form factor devices;
f) device connector capable of mating with both backplanes and cables;
g) an electrically balanced design that reduces EMI and crosstalk;
h) and a measurement scheme focusing on interoperability at separable connectors without requiring any internal physical access.

1.2 SSA family of standards

The relationships of the SSA family of standards is illustrated in Figure 1.

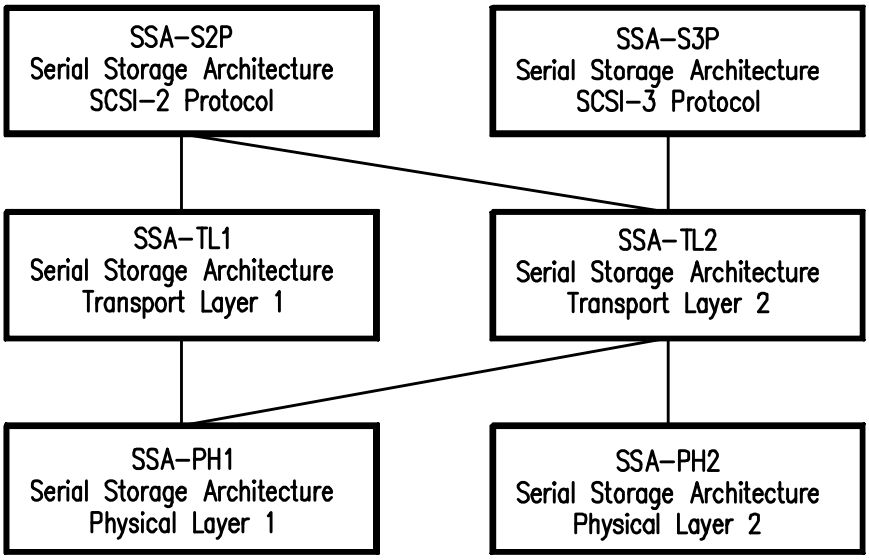

Figure 1 - Relationship of the SSA standards

1.2.1 SSA-S2P

Serial Storage Architecture - (SSA-S2P) SCSI-2 Protocol defines the SCSI-2 Protocol used to run on top of the SSA transport layers 1 or 2.

1.2.2 SSA-S3P

Serial Storage Architecture - (SSA-S3P) SCSI-3 Protocol defines the SCSI-3 Protocol used to run on top of the SSA transport layer 2.

1.2.3 SSA-TL1

Serial Storage Architecture - (SSA-TL1) Transport Layer 1 defines the Transport layer that runs SSA-S2P and runs on SSA-PH1.

1.2.4 SSA-TL2

Serial Storage Architecture - (SSA-TL2) Transport Layer 2 defines the Transport layer that runs SSA-S2P and SSA-S3P and run on SSA-PH1 or SSA-PH2.

1.2.5 SSA-PH1

Serial Storage Architecture - (SSA-PH1) Physical Layer 1 defines the Physical layer that runs SSA-TL1 and SSA-TL2, and consists of the electrical characteristics of the interface and the connectors.

1.2.6 SSA-PH2

Serial Storage Architecture - (SSA-PH2) Physical Layer defines the Physical layer that runs SSA-TL2, and consists of the electrical characteristics of the interface and the connectors.

2 References

2.1 Normative references

The following standards contain provisions which, through reference in SSA-PH2, constitute provisions of this standard. At the time of publication, the edition indicated was valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standard listed below. Members of IEC and ISO maintain registers of currently valid International Standards, and ANSI maintains registers for American National Standards.

T10.1 / 1147 - *Information Technology - Serial Storage Architecture - Transport Layer 2 (SSA-TL2)*

ANSI/EIA 364 - *Electrical Connector/Socket Test Procedures Including Environmental Classifications.* December 1994 revision C - parts 13, 20, 21, 23, 31, 41 and 46

IEC 512: - *Electromechanical components for electronic equipment; basic testing procedures and measuring methods*

IEC 512-2 (1985) *Part 2 - Insulation resistance*, 22 pp. (April 92) TC 48

IEC 512-4 (1976) *Part 4 - Dynamic stress tests*, 15 pp. Code H (First edition) TC 48

IEC 512-5 (1992) *Part 5 - Impact tests (free components), static load tests (fixed components), endurance tests and overload tests*, 43 pp. Code S (Second edition) TC 48

IEC 512-6 (1984) *Part 6 - Climatic tests and soldering tests*, 53 PP- Code U (Second edition) TC 48

IEC 512-7 (1993) Part 7 - *Mechanical operating tests and sealing tests*, 33 PP Code O (Third edition)

IEC 512-11-7 (1996) *Part 11 - Climatic tests - Test 11g: Flowing mixed gas corrosion test* (First edition)

IEC 801 - *Environmental testing*, 1988

Editor s note: This clause will be adjusted at time of publications to reference appropriate standards.

2.2 Informative references

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X3.293:1996 - *Information Technology - Serial Storage Architecture - Physical Layer 1 (SSA-PH1)*

X3.295:1996 - *Information Technology - Serial Storage Architecture - Transport Layer 1 (SSA-TL1)*

X3.294:1996 - *Information Technology - Serial Storage Architecture - SCSI-2 Protocol (SSA-S2P)*

T10.1 / 1051 - *Information Technology - Serial Storage Architecture - SCSI-3 Protocol (SSA-S3P)*

Further information regarding the implementation of this standard may be available at http://www.ncits.org/t10 or http://www.ssaia.org.

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3 Definitions, symbols and abbreviations

3.1 Definitions

3.1.1 application: A process that is communicating via the link**.**

3.1.2 Cable: A uniform media between connectors containing the four conductors required for two lines.

3.1.3 Cable Assembly: A cable with connectors, backshells and retention schemes on each end.

3.1.4 character: A sequence of 10 encoded bits that represents a data byte or a protocol function.

3.1.5 Complex port connection: Any means of connecting ports other than a single cable assembly

3.1.6 frame: A sequence of 4 or more data characters surrounded by FLAG characters.

3.1.7 Line: The pair of balanced electrical conductors connecting (1) the positive side of the line driver port connector to the positive side of the line receiver port connector and (2) the negative side of the line driver port connector to the negative side of the line receiver port connector.

3.1.8 Line+: The line conductor connecting the positive side of the line driver port connector to the positive side of the line receiver port connector.

3.1.9 Line-: The line conductor connecting the negative side of the line driver port connector to the negative side of the line receiver port connector.

3.1.10 Line Driver: The electrical circuitry that set the logical state of the line at the port connector.

3.1.11 LineIn+: The line receiver connection to the Line+ conductor.

3.1.12 LineIn-: The line receiver connection to the Line- conductor.

3.1.13 LineOut+: The line driver connection to the Line+ conductor.

3.1.14 LineOut-: The line driver connection to the Line- conductor.

3.1.15 Line Receiver: The electrical circuitry that detect the logical state of the line at the port connector including Line Segment Termination. The Line Receiver shall be capable of reporting bit errors.

3.1.16 Line Segment: That portion of a Line between Line Driver and the Line Segment termination.

3.1.17 Line Segment termination: The electrical properties of the load on the end of the line segment opposite the end associated with the Line Driver.

3.1.18 Link: The serial connection between ports on two devices including the Line Drivers, Line Receivers, and the associated Cable Assembles.

3.1.19 node: A system, controller or device with one or more ports.

3.1.20 Port: A line driver and a line receiver operating together on a device (two lines, four conductors).

3.1.21 Port connection: The combination of two lines that tie the line driver in a port to the line receiver in the another port and the line driver in the other port to the line receiver in the first port.

3.1.22 Port connection coupler: A device that ties two port connection segments together.

3.1.23 Port connection segment: A portion of a port connection that ties a line driver to a line segment termination on one line and a line driver to a line segment termination in the other line.

3.2 Symbols and abbreviations

AWG American wire gauge
BER bit error rate.
CMOS complementary metal oxide semiconductor.
CRC cyclic redundancy check.
CUT connector under test
DMA direct memory access
DUT device under test
EMI electro-magnetic interference
ERP error recovery procedure
ESD electro-static discharge
FCS fiber channel standard
FDDI fiber distributed data interface
FSN frame sequence number
HSSDC high speed serial data connector
IDC insulation displacement connector

LED Light Emitting Diode
LFT Line Fault Threshold
LSI large scale integration
NRZ non-return-to-zero
PCC Port Connection Coupler
POR power-on reset
POST power-on self-test
RAS reliability, availability and serviceability
RFI radio-frequency interference
RH relative humidity
RLFT Receiver Line Fault Threshold
RSN receive sequence number
SCSI Small Computer Systems Interface
SSA Serial Storage Architecture
TSN transmit sequence number
SMS SSA Message Structure
$\mathbf{V_{it}}$ Voltage of LineIn termination
$\mathbf{V_{ot}}$ Voltage of LineOut termination
& Logical AND
= Assignment or comparison for EQUAL
≠ Comparison for NOT EQUAL
< Comparison for LESS THAN
≤ Comparison for LESS THAN OR EQUAL TO
> Comparison for GREATER THAN
+ ADD
- SUBTRACT
* MULTIPLY
± PLUS OR MINUS
≈ APPROXIMATELY
» MUCH GREATER THAN

4 Conventions

Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the glossary or in the text where they first appear. Lower case is used for words having the normal English meaning.

Fields containing only one bit are usually referred to as the "named" flag instead of the "named" field. When a bit is set its value is 1. When a bit is cleared, its value is 0.

Numbers that are not immediately followed by lower-case "b" or "h" are decimal values. Numbers immediately followed by lower-case "b" (xxb) are binary values. Numbers immediately followed by lower-case "h" (xxh) are hexadecimal values. Decimal numbers are indicated with a comma (e.g., two and one half is represented as "2,5). Decimal numbers having a value exceeding 9999 are represented with a space (e.g., 2345 and 12 345).

In circuit diagrams, a T intersection implies a connection, a + implies no connection, and a + with a dot at the crossover implies a connection.

In case of conflict, figures take precedence over tables, and both figures and tables take precedence over text.

5 Modulation

The encoded data is transmitted as a base-band digital signal using the non-return-to-zero (NRZ) method.

6 Data Rate

SSA links operate at a data rate of either 40 MB/s (i.e., 400 Mb/s) or 20 MB/s (i.e., 200 Mb/s) on the line.

The transmit clock shall be accurate to ± 250 PPM.

The receiver shall acquire bit synchronization from the transitions in the transmitted data. If an asynchronous sampling technique is used then the design shall take metastability into account.

7 Electrical requirements

SSA may be implemented with a number of different physical schemes. In this standard only the AC coupled copper version is defined. Future standards may define alternate media and electrical interfaces. The requirements apply to both internal and external interconnections (except that the shielding requirements do not apply for internal).

Table 1 shows the physical schemes that are compatible with the SSA protocol.

Table 1 - SSA physical interconnect schemes

Physical Scheme	Internal	External
Directly coupled copper	SSA-PH1	SSA-PH1
AC coupled copper	This standard	This standard

NOTE 1 - The AC coupled scheme specified in this standard is compatible with devices implemented using the SSA-PH1 standard directly coupled copper scheme, if the SSA-PH1 receiver input range includes V_{it} ± 650 mV.

The electrical configuration of the serial link is shown in Figure 2.

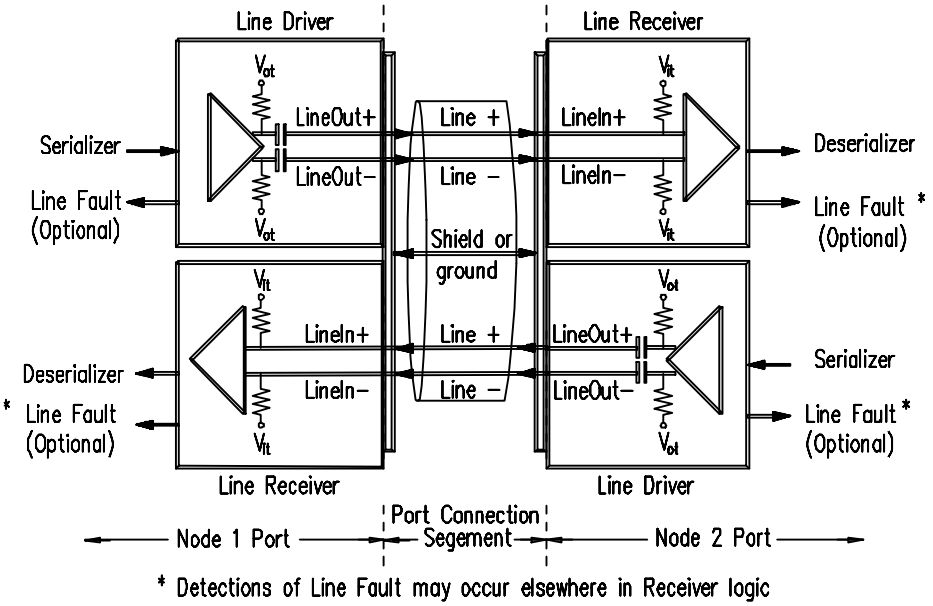


Figure 2 - Electrical configuration for SSA serial links

The electrical requirements are defined in a modular way so that each of the three basic components of the serial link are individually defined. The three basic components are the Line Driver, Port Connection, and the Line Receiver. The boundaries of these components are chosen so that the requirements apply at the separable connectors on the ports.

In order to minimize transmission line reflections the characteristic impedance measured at the LineIn+ and LineIn- pins shall meet the requirements in 7.3, the characteristic impedance measured at LineOut+ and LineOut- shall meet the requirements of 7.1.5.1, and the characteristic impedance of the Port Connection shall meet the requirements of 7.5. This measurement is affected by the details of the electrical path between the device connector pins and the terminating resistor near the receiver.

The test conditions defined create an electrical environment that approximates worst case noise and loading. In order to present a more complete noise exposure, specific activity on ports not directly under test is also required during the test execution. These test conditions reveal degradation caused by improper stubs, excessive cross talk, excessive series inductance, inadequate decoupling and other effects that may be caused by inappropriate design.

The test points that apply are shown in Figure 3. The Line Driver requirements are verified at M1. Inputs to verify the line requirements are measured at M2. Outputs for the Line requirements are verified at M3. Inputs to verify the Line Receiver characteristics are verified at M4.

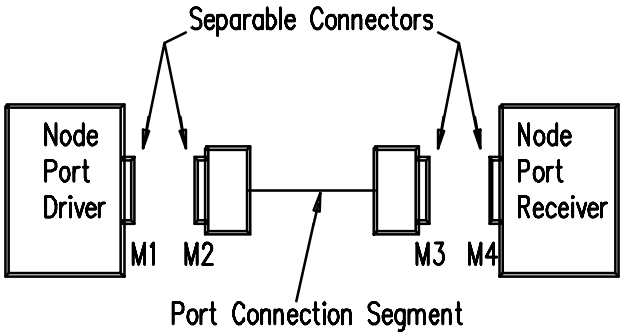


Figure 3 - Test points

In order to assist inter-operability between ports designed or manufactured under different conditions, the Line Driver, Port Connection, and Line Receiver shall each satisfy their respective requirements. See 7.5 for requirements applying to complex lines, including Lines using repeaters, equalizers, and other non-homogeneous schemes between M2 and M3.

The overall performance requirement on the system is a bit error rate less than 10^{-12} (e.g., less than one error in 10^{12} bits transferred). In order to allow for system noise not present during the Line Receiver requirements test, the Line Receiver itself shall not exceed a bit error rate of 10^{-13} with the defined inputs (see 7.2.4) at M4.

The pulses and waveforms are defined in terms of the differential voltage observed at specific points with specific loads, even though SSA uses current drivers. Measuring the required differential currents is beyond the present state of the measurement art. All references to timing are made with respect to the differential voltage signals.

7.1 Line driver

7.1.1 General description

An SSA line driver is a circuit that converts logic signals from the serializer into differential currents to drive the outbound lines.

The SSA line driver shall deliver balanced currents to the line. Balance is achieved when the di/dt in the Line+ conductor is identical in magnitude but opposite in sign to the di/dt in the Line- conductor at the same point in time and space. Current balance is needed to keep the signal return currents off the external shield (for EMI reasons) and away from the other SSA signal paths in the cable (for cross talk reasons). The amount of imbalance that is tolerable is not defined in this standard because the cross talk effects are covered by the requirements on the Line Drivers, Port Connection, and Line Receivers. The EMI effects are dependent on the system configuration and the interconnect shielding used.

To ensure balanced currents from the Line Driver, the Line Driver shall contain a single current source (sink) whose output shall be connected to the Line Driver internal Load and the internal Coupling Element, and shall directed to Line+ through the LineOut+ connection and to Line- through the LineOut- connection in such a manner that the sum of the currents in both lines nominally equals half the current source output at all times. The total current (current source output) is nominally 19 mA d.c. and is designated I_t. The current in Line+ is designated I_+ and the current in Line- is designated I_-. Nominally $I_t = (I_+ + I_-)/2$ which requires a balanced condition, $dI_+ / dt = - dI_- / dt$.

The Line Driver shall have sufficient voltage conformance to accommodate ground shift between the two ports (see 7.4).

Figure 4 shows one possible implementation of a Line Driver. The current source output is distributed to the line using the N channel transistors. Notice that even if the properties of the transistors or of the signals driving the transistor gates are not identical that the balance condition still exists on the line.

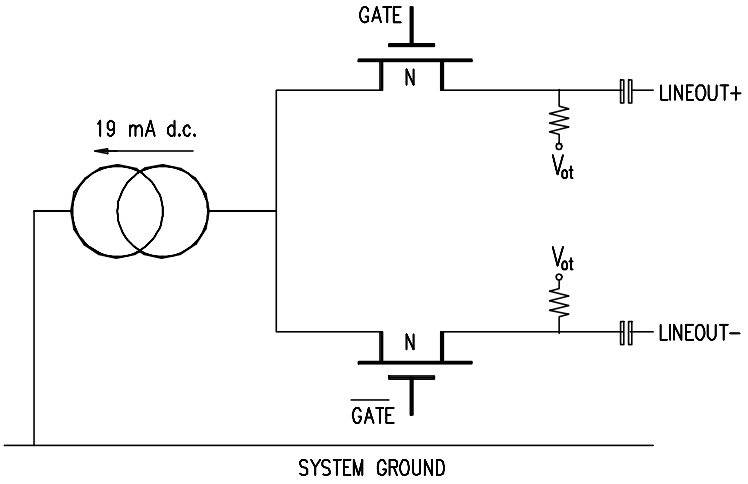


Figure 4 - SSA Line Driver implementation example

The properties of these current steering transistors and their control signals need to be carefully controlled to meet other driver requirements such as slew rate, spectral content and jitter.

In general, balanced transmissions are aided by ensuring that the properties of Line+ are identical to the properties of Line-.

Figure 5 shows the relationship of the currents existing during signal transitions. Transmission is balanced if mirroring through the mirror plane shows no new traces. Time skew produces significant imbalance.

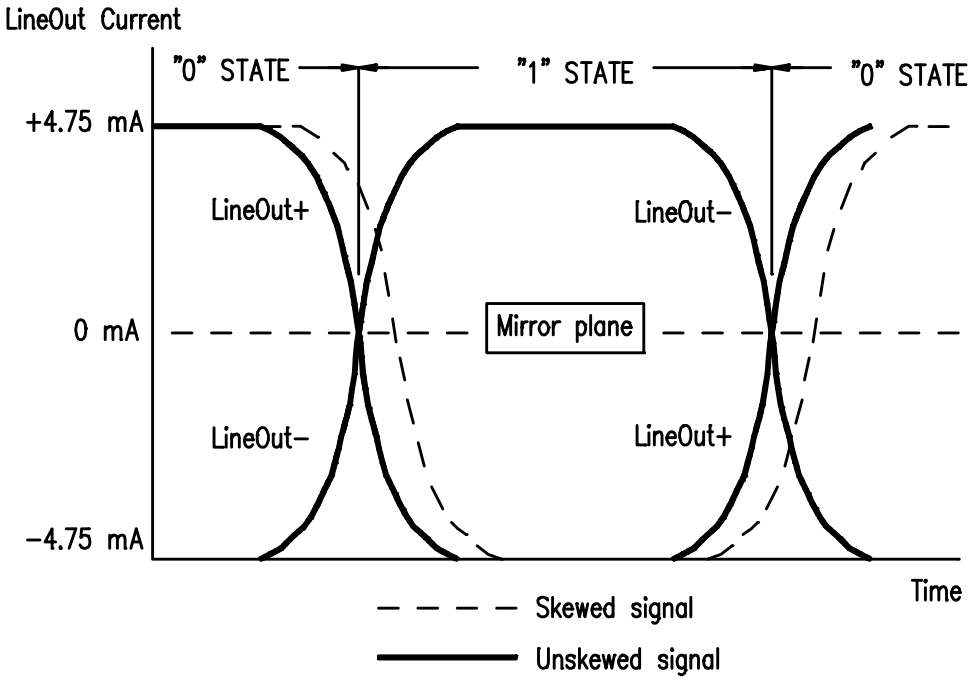


Figure 5 - Relationship between LineOut currents at the port connector

7.1.2 Test conditions for line drivers

All Line Driver measurements are referenced to the Port Connector.

7.1.2.1 General requirements

Line drivers shall be tested using the test circuit shown in Figure 6. The distance between the port connector and the load resistance LR (labeled X in Figure 6) shall not exceed 5 cm. The distance between the measurement point (at the LR and MR junction) and the load resistance LR (labeled Z in Figure 6) shall not exceed 5 mm. The difference between the connector to measurement point distance (labeled Y in Figure 6) of the LineOut+ and LineOut- lines of the driver shall not exceed 5 mm. The resistance of the combined load resistance LR and measurement resistance MR shall be 75 $\Omega \pm 2\%$. The total additional capacitive load from the scope probing scheme between Line+ and ground and between Line- and ground at the port connector shall be a maximum of 1,5 pF. This capacitance includes the sensing probes and equipment added to enable probing. The load shall conform to the characteristic impedance requirements in 7.3 at its connector.

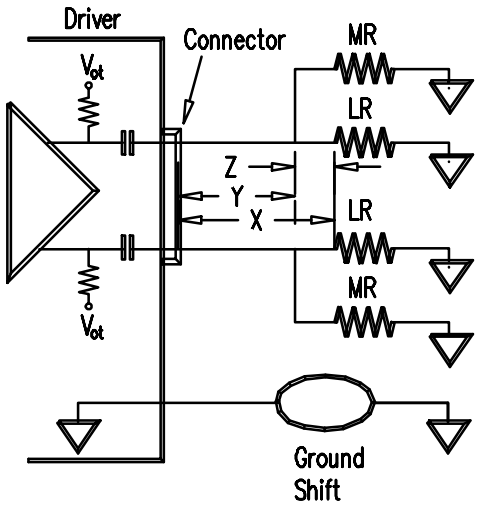


Figure 6 - Test environment for drivers

The measurement procedure shall be performed as follows.

a) The measurement system bandwidth including preamplifier and probes shall be adequate for the 5th harmonic of the highest frequency square wave.

b) Trigger on the rising edge of single ended true (logical 1) output with a minimum of 5 and a maximum of 35 data bit times delay after the trigger edge prior to the measurement. This delay is required to capture data dependent jitter caused by intersymbol interference. This test returns twice the actual jitter due to the data edge triggering. The actual jitter value (half that measured above) shall be used when determining conformance.

c) Driver waveform shall be measured as a differential voltage with an accuracy of ±10 mV.

The data pattern shall consist of continuous contiguous K28.5 characters resulting in a character stream with alternating running disparity. This pattern contains maximum and minimum run lengths (both high and low) and therefore is a worst case pattern. All SSA ports shall be capable of running this pattern continuously. A mechanism shall be implemented in all SSA ports to enable the continuous contiguous K28.5 transmissions required for these tests at all supported speeds.

The test environment shall include electrical activity on the device typical of the intended applications environment. All ports on the node shall be active during the driver test. Continuous K28.5 characters shall be presented to the receive side of the port used for the driver test. All inputs should originate from drivers that conform to this standard.

7.1.2.2 Driver jitter

The maximum allowed Line driver jitter is defined in 7.1.4. The line driver jitter shall be measured under the test conditions defined in 7.1.2. The jitter shall be measured at the zero differential voltage level as a peak to peak value for the population sampled. The maximum value for this measured jitter (due to the triggering method) is twice the actual jitter defined in Table 5.

7.1.2.3 Driver slew rate

The maximum allowed driver slew rate is defined in 7.1.4.

The line driver slew rate shall be measured under the conditions defined in 7.1.2.1 and as follows:

a) measurement system bandwidth sufficient to measure the slew rate defined in 7.1.4;

b) slew rate of the most probable curve from multiple samples of the waveform between ±200 mV differential voltage levels.

7.1.2.4 Line driver output spectral content

The line driver output spectral content shall be measured under the test conditions defined in 7.1.2.1 with the following changes;

a) the load shall consist of the circuit shown in Figure 7 and shall conform to 7.3;
b) the capacitive load to logic ground on each side of the driver port shall be minimized and shall be less than 2 pF;
c) the ground shift shall consist of -0,5 V d.c. to +0,5 V d.c. only;
d) both the LineOut+ and LineOut- shall be independently measured (Figure 7 shows the measurement of only one LineOut).

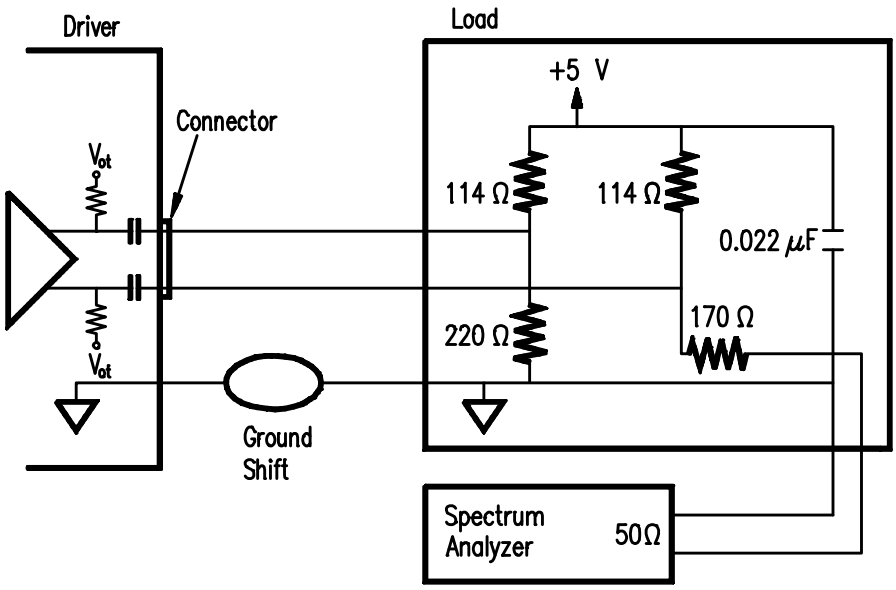


Figure 7 - Test environment for driver spectral content

The maximum allowed line driver output spectral content is defined in 7.1.4.

The line driver output spectrum shall be within the shaded area of Figure 9 using the data points from Table 2 using a detection bandwidth of 10 kHz over the frequency range d.c. to 1,0 GHz for the 200 Mb/s speed and d.c. to 1,5 GHz for the 400 Mb/s speed. The envelope of the measured spectrum shall be used to determine the intensity of the spectral content as shown in Figure 8.

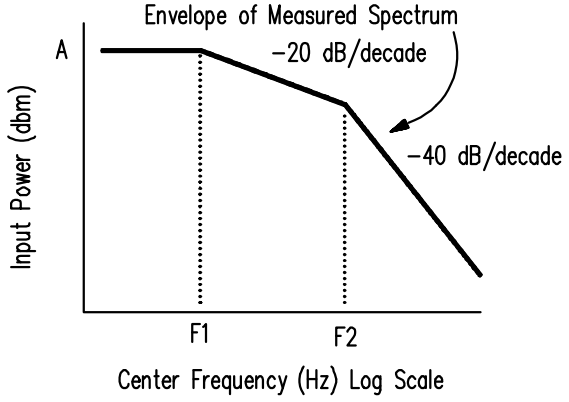


Figure 8 - Driver output spectral content

Table 2 - Driver output spectral content

Speed	F1	F2	A
400 Mb/s	160 MHz	636 MHz	-11 dBm
200 Mb/s	80 MHz	318 MHz	-11 dBm

7.1.3 Pulse mask for SSA drivers

The differential voltage measured using the test circuit, measurement equipment, data patterns, and test environment defined in 7.1.2 shall remain outside the shaded area and be wholly contained between the V2 and -V2 voltage levels of the pulse mask shown in Figure 9.

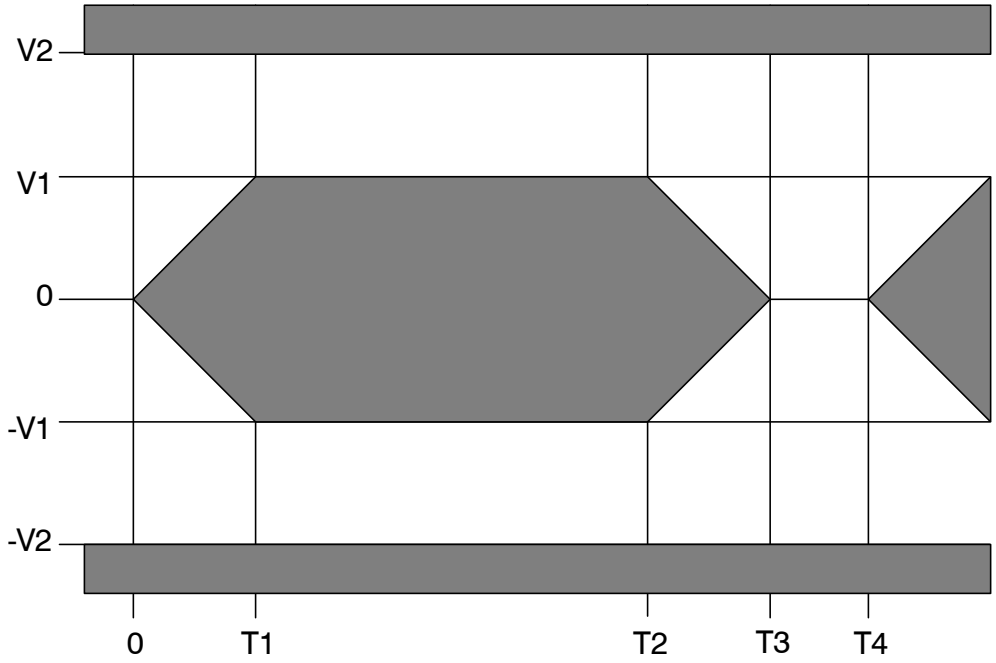


Figure 9 - SSA driver pulse mask

Table 3 contains the requirements when triggering from the source clock.

Table 3 - Driver system operating parameters

Speed	V1	V2	T1	T2	T3	T4
400 Mb/s	500 mV	1000 mV	0,25 ns	2,05 ns	2,30 ns	2,50 ns
200 Mb/s	500 mV	1000mV	0,25 ns	4,47 ns	4,72 ns	5,00 ns

Table 4 contains the requirements when triggering as specified in 7.1.2.1.

Table 4 - Driver test parameters

Speed	V1	V2	T1	T2	T3	T4
400 Mb/s	500 mV	1000 mV	0,25 ns	1,85 ns	2,10 ns	2.50 ns
200 Mb/s	500 mV	1000mV	0,25 ns	4,19 ns	4,44 ns	5,00 ns

7.1.4 Line driver operating requirements

The operating requirements for the line driver are summarized in Table 5.

Table 5 - Line driver operating requirements at the port connector

Line driver requirements:	**minimum**	**nominal**	**maximum**
Output current peak to peak (s)	8,1 mA	9,5 mA	10,9 mA
Output current imbalance (LineOut+ - LineOut-) (s)	-0,5 mA		+0,5 mA
Off state output d.c. current (s)	-25 μA		+25 μA
LineOut+ leakage current to ground			10 μA d.c.
LineOut- leakage current to ground			10 μA d.c.
Output termination voltage (V_{ot})	2.97V		5.5 V
a.c. component of V_{ot} (peak to peak) as measured from Logic Ground to V_{ot}.			100 mV from 30 Hz to 6 MHz 50 mV from 6 MHz to 500 MHz
Output voltage slew rate (d)	2,0 V/ns		5,0 V/ns
Output jitter at 200 Mb/s (peak-peak) [1] (d)			0,28 ns
Output jitter at 400 Mb/s (peak-peak) [1] (d)			0,20 ns
Output voltage spectral content (s)	Shall be within the envelope (see Figure 8) under the test conditions defined in 7.1.2.4		
Output voltage waveform (d)	Shall be within pulse mask (see Figure 9) under test conditions defined in 7.1.2		
Ground shift	Shall comply with 7.4		
NOTE [1] - This is an operating requirement. It is the actual jitter allowed under system operating conditions. It is not the result of the tests defined in 7.1.2 because of the triggering scheme used for these tests. The test conditions in 7.1.2 result in the observed jitter being twice the value defined in this table. (s) = single ended, (d) = differential			

Drivers shall tolerate single ended voltage inputs from -0,5 to +4,13 V applied through 75Ω ±1% without damage in a power off state. The 4,13 V level is derived from the 3,63 V level (Table 9) plus 0,5 V ground shift.

7.1.5 Other Line Driver requirements

Figure 10 illustrates the schematic of the Line Driver termination.

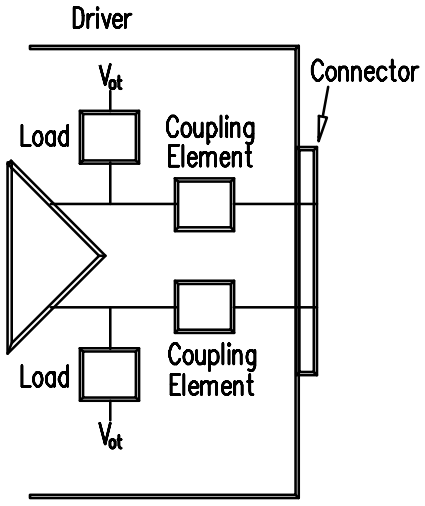


Figure 10 - Line Driver termination schematic

7.1.5.1 Line Driver termination

The Line driver termination is defined in terms of TDR impedance in the same way as Line Segment termination except it is measured at the Port connector LineOut pins (see 7.3). Table 6 specifies the Line Driver termination requirements.

Table 6 - Electrical requirements for Line Driver termination

Receiver port test configuration	TDR rise time max (ps)	Zo max (Ωs)	Zo min (Ωs)
LineOut+ to logic ground	375	90	60 [1]
LineOut- to logic ground	375	90	60 [1]
LineOut+ to LineOut-	375	180	120 [1]
[1] A single excursion below this limit shall be allowed for a maximum of 0,75 ns			

7.1.5.2 Line Driver internal load

Each Line Driver internal load is a resistor with a d.c. impedance of 75 Ω ± 1% connected between the internal coupling element and V_{ot} as shown in Figure 10.

7.1.5.3 Line Driver internal coupling element

The Line Driver internal coupling element is an element that is capacitive at 20 MHz and has a maximum impedance of 10 W over a frequency range of 20 MHz to 500 MHz. Any self resonant frequency shall occur above 75 MHz. For example, this may be achieved with a 1 nF ± 20% capacitor which meets the Line Driver coupling element requirements.

7.2 Line receiver

7.2.1 General description

The line receiver is a circuit that converts the differential voltage on the inbound line into a logic signal. When the line is terminated per 7.3 the input signal levels are as shown in 7.2.6.

7.2.2 Receiver line fault detection

The line receiver may indicate a line fault when certain line conditions exist. These conditions are left to the implementer to determine.

Reporting of line faults is a function of the transport layer (see SSA-TL2).

NOTE 2 - An example of fault detection in a Line Reciever is shown in informative Annex F.

7.2.3 Test conditions for receivers

Line receivers shall be tested using the test circuit shown in Figure 11. Line Receiver input measurements shall be made at the port connector associated with the Line receiver. The distance between the line receiver port connector and the line driver is not defined. The capacitive load of the sensing probes and related equipment shall not exceed 2 pF.

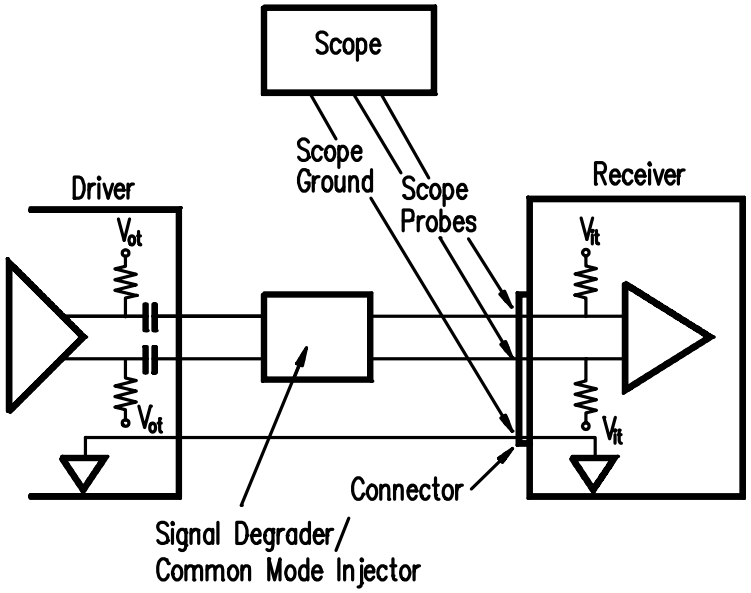


Figure 11 - SSA receiver test environment

These tests measure the line receiver's maximum error rates with the input signals shown in Figure 12.

The test environment shall include electrical activity on the node typical of the intended application environment. All ports on the node shall be active during the receiver test. Valid SSA traffic shall be present in the driver side of the port used for the receiver test. All line receiver inputs shall originate from line drivers that conform to 7.1. Electrical activity of the node should be representative of the normal operation of the node in a heavily loaded system during this test.

The measurement requirements are:

a) The measurement system bandwidth including preamplifier and probes shall be adequate for the 5th harmonic of the highest frequency square wave.

b) Trigger on rising edge of single ended true (logical 1) output with a minimum of 5 and a maximum of 35 data bit times delay after trigger edge prior to measurement. This delay is required to capture data dependent jitter caused by intersymbol interference. Note that this test returns twice the actual jitter due to the data edge triggering. The actual jitter (half that measured above) shall be used when determining conformance with the receiver requirement.

c) Input waveform shall be differential voltage.

d) Voltage measurement accuracy ±10 mV.

The data pattern shall allow for synchronization and the detection and reporting of errors.

The amplitude and jitter appearing at the line receiver port connector (using the above measurement requirements) shall be adjusted with a signal degrader or common-mode injector circuit or other appropriate means to match the boundaries of the pulse mask defined in 7.2.4 as closely as possible at all required common mode input levels. The required common mode levels are defined in Table 9. The adjustment procedure is left to the implementer. Annex G describes a method for degrading the amplitude and injecting controlled common mode levels. The scope probes (or equivalent electrical loads) shall be left in place during the recording of the receiver error detections to ensure that the input conditions are met during the error recording. When using the signal degrader, operation shall be maintained such that the error detection and reporting mechanisms function correctly. The validity of the observed input conditions shall be checked by substituting continuous contiguous K28.5 characters for the data pattern that will be used for the test and applying the method detailed in Annex E.

The receiver pulse mask shall be recorded during error free operation. The node shall be capable of detecting and reporting errors.

The test duration shall be sufficient to verify the maximum bit error rates defined in 7.2.6.

7.2.4 Pulse mask for SSA receiver input signals

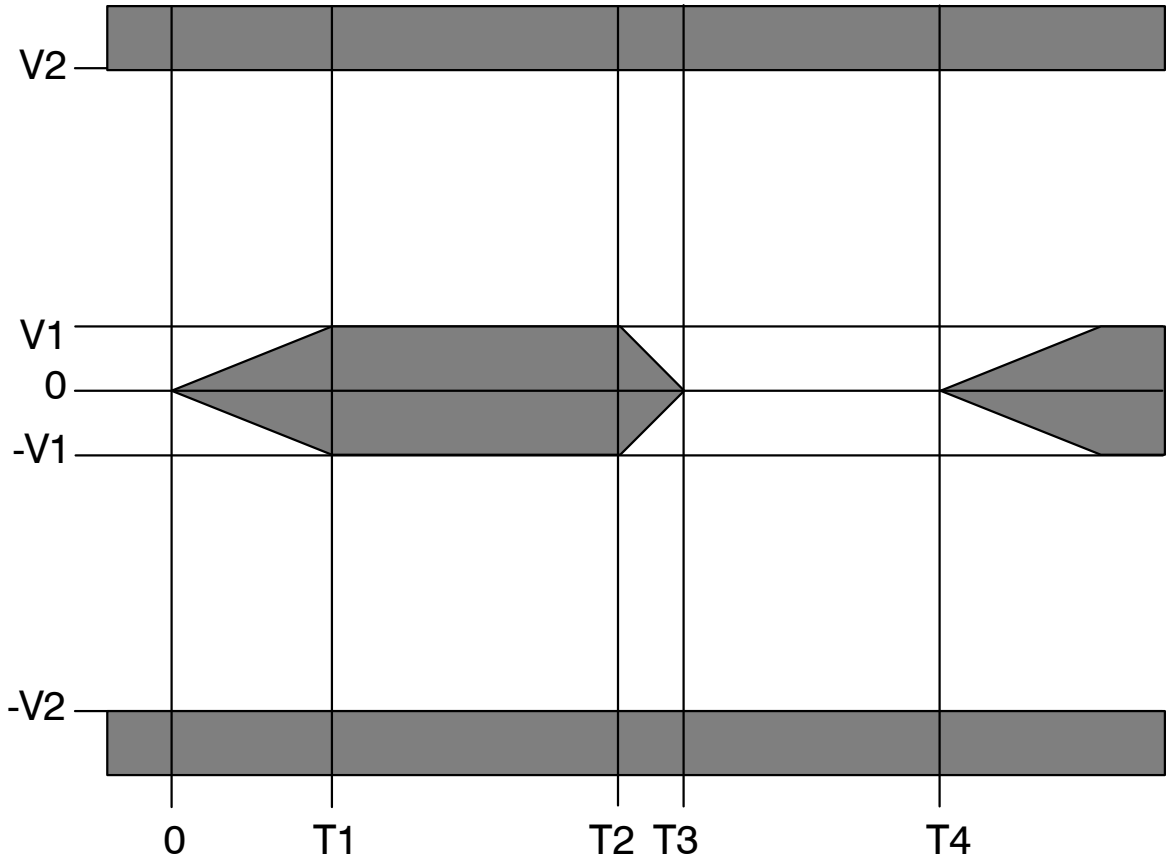


Figure 12 - Receiver pulse mask

Table 7 contains the requirements when triggering from a source clock.

Table 7 - Receiver system operating parameters

Speed	V1	V2	T1	T2	T3	T4
400 Mb/s	100 mV	1000 mV	0,500 ns	1,425 ns	1,677 ns	2,500 ns
200 Mb/s	200 mV	1000 mV	1,000 ns	2,850 ns	3,350 ns	5,000 ns

Table 8 contains the requirements when triggering as specified in 0.

Table 8 - Receiver test parameters

Speed	V1	V2	T1	T2	T3	T4
400 Mb/s	100 mV	1000 mV	0,500 ns	0,600 ns	0,850 ns	2,500 ns
200 Mb/s	200 mV	1000 mV	1,000 ns	1,200 ns	1,700 ns	5,000 ns

7.2.5 Line receiver common mode input requirements

Due to common node noise coupled into the SSA environment from external sources it is necessary for the line receiver to accommodate common mode input voltages. These levels are defined in Table 9.

7.2.6 Line receiver operating requirements

The operating requirements for the line receiver are summarized in Table 9.

Table 9 - Receiver operating requirements at the port connector

Line receiver requirement:	Minimum	Maximum	Notes:
Differential Input Voltage at 400 Mb/s	±100 mV	±1000 mV	Peak Differential. See pulse mask 7.2.4
Differential Input Voltage at 200 Mb/s	±200 mV	±1000 mV	Peak Differential. See pulse mask 7.2.4
Input Termination Voltage (V_{it})	2,97 V d.c.	3,63 V d.c.	The a.c. component (peak to peak) as measured between both LineIn+ and LineIn- to logic ground at the port connector shall not exceed 50 mV.
Single ended Input level (LineIn+ and LineIn-)	V_{it} - 0,65 V	V_{it} + 0,65 V	
a.c. component of the common mode voltage	V_{it} - 0,15 V V_{it} - 0,05 V	V_{it} + 0,15 V V_{it} + 0,05 V	0 to 6 MHz 6 MHz to 500 MHz
Bit error rate at minimum input pulse mask over required common mode input levels	0	10^{-13}	Test performed according to 0 and 7.2.4

NOTE 3 - The line receiver input voltage sensitivity (the minimum differential input voltage that causes the line receiver to detect a logic transition) shown in Table 9 may be reduced below the 100 mV or 200 mV maximum. The lower this sensitivity voltage the greater the receiver noise margin. Receiver hysteresis is not required nor recommended.

7.3 Line segment termination

Line Segment termination is the electrical properties of the load on the end of the line segment opposite the end associated with the Line Driver.

Ideally a lossless, stubless transmission line that matches the media in the line exists between the port connector and a purely resistive matching terminating element. Ideally the receiver chip connects with no capacitance and no stub to this transmission line. It is necessary to approximate this ideal condition to avoid reflections on the line. Therefore a performance requirement requiring characteristic impedance levels at the line receiver port connector is used.

In order to accommodate the current levels and conformance voltage levels from the driver, the d.c. input characteristics for LineIn+ and LineIn- shall appear as a 75 Ω ± 1% resistor connected to +3,3 V ± 10% (see Figure 6). The line segment termination shall tolerate a direct short to -0,5 V for indefinite periods.

The characteristic impedance (Zo) measured into the LineIn+ and LineIn- pins of the connector with a Time Domain Reflectometer (TDR) shall meet the requirements in Table 10 including all time points affected by the connector and all associated electrical paths. The test environment shall reflect the conditions existing during operation.

Table 10 - Electrical requirements for line segment termination

Receiver port test configuration	TDR rise time max (ps)	Zo max (Ωs)	Zo min (Ωs)
LineIn+ to logic ground	375	90	60 [1]
LineIn- to logic ground	375	90	60 [1]
LineIn+ to LineIn-	375	180	120 [1]
NOTE [1] - A single excursion below this limit shall be allowed for a maximum of 0,75 ns			

7.4 Ground shift

The system environment shall guarantee that the maximum instantaneous ground shift between a line driver and the associated line segment termination is 0,5 V (peak to peak) from d.c. to 6 MHz and 0,1 V (peak to peak) from 6 MHz to 500 MHz when the link is operating. To avoid circuit damage instantaneous ground shift shall never exceed 2,0 V when any line segment is connected.

The a.c. component of the voltage difference between frame ground and logic ground of any node shall not exceed 200 mV from the frequency range of 0 to 6 MHz, and shall not exceed 100 mV from the frequency range of 6 MHz to 500 MHz.

Conditions may exist where there are no line receivers (with ability to report error rate) but line segment termination is present (for example with repeaters). In this case, the ground shift is measured between the logic ground of the driver and the ground connection of the 3,3 V source used to supply the line segment termination. Multiple line segments may exist within the line. Each line segment shall be treated independently with respect to ground shift.

Figure 13 specifies the measurement position for ground shift. The conditions for this measurement should be

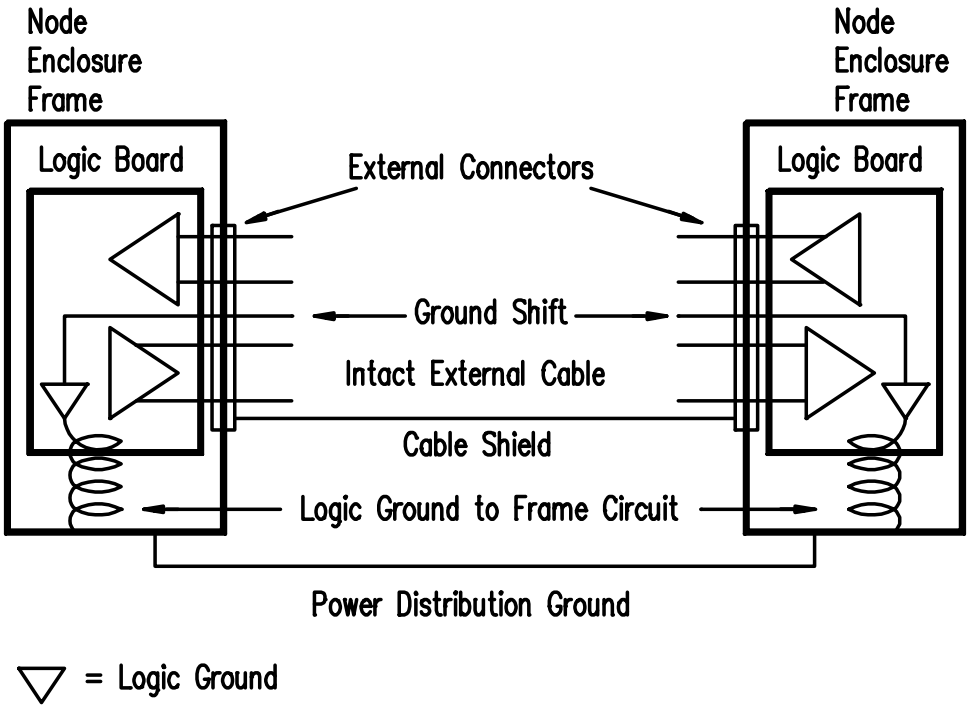


Figure 13 - Definition of ground shift

representative of the normal operation of the node in a heavily loaded system.

7.5 Port connection

A port connection provides the means for connecting two ports together. Port connections are formed from two lines. Each line shall consist of the means for connecting line drivers to line receivers as shown in Figure 14. Each line shall consist of one or more line segments as shown in Figure 14. If only cable assemblies are used to implement the lines there is only one line segment between the line driver and the line receiver. This applies even if there is passive equalization built into one or more of the cable assemblies.

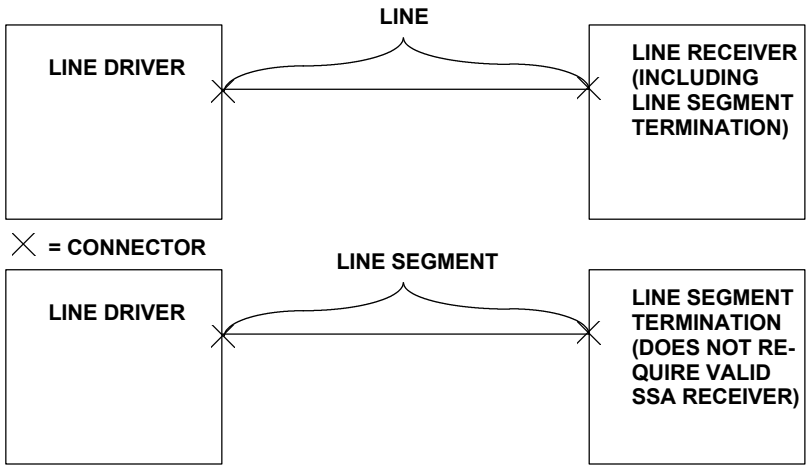


Figure 14 - Lines and line segments

A line segment is the part of a line between a driver and its directly connected line termination.

Line segments shall conform to the ground shift requirements in 7.4 and shall connect to valid line segment termination (see 7.3).

The Lines shall have a differential characteristic impedance of 150 Ω ± 10% when measured with a TDR with 375 ps rise time. This includes the media, connectors, and the backshell areas of the cable assemblies.

Anything in the line segment between drivers and its associated line segment termination (such as equalizer circuits, changes in media construction, and series connectors) shall appear as balanced 150 Ω transmission lines to the driver side and shall not increase the d.c. conformance voltage requirements for the drivers. The tolerance on the characteristic impedance and the measurement technique shall be the same as for the uniform media used in the line segment. These non-media entities are expected to reduce the signal amplitude but may be useful in reducing jitter or for using multiple cable assemblies in the same segment.

Figure 15 shows the structure of port connections and port connection segments. A port connection shall have two lines that provide the means for transmitting electrical signals between line drivers and line receivers.

A port connection segment consists of two line segments. A port connection contains one port connection segment if only cable assemblies, including those with passive equalization, are used to implement the port connection. A port connection segment may contain multiple cable assemblies with or without passive equalization.

Only one connector of a Port Connection Segment (PCS) may source power to the Port Connection Segment.

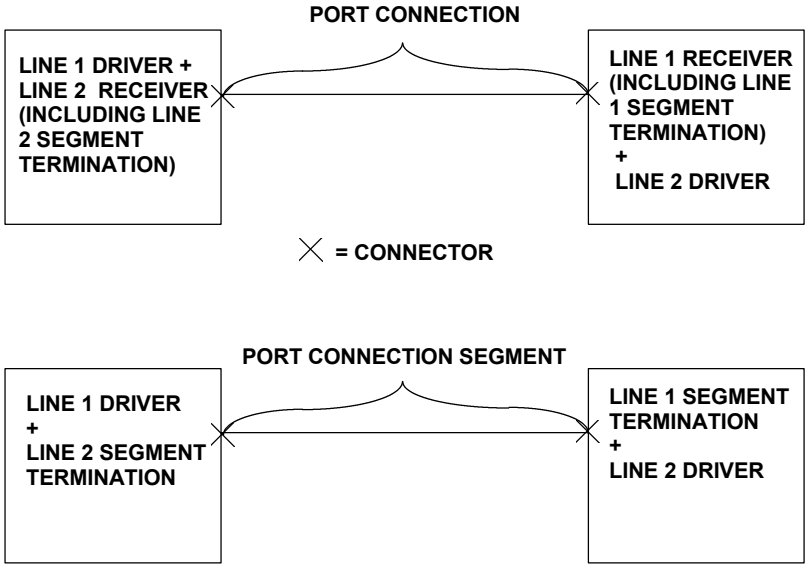


Figure 15 - Port connection and port connection segments

7.5.1 Test environment for port connection segments

The port connection segment test shall use point (M2) for the input signal and point (M3) for the output (see Figure 3, Figure 6 and Figure 10). The input signal at M2 shall be degraded using a signal degrader to match the minimum pulse mask for the driver (see 7.1). K28.5 characters (see SSA-TL) shall be used throughout this test. The output signal at M3 shall be measured and compared with the receiver pulse mask in 7.2 using the method defined in Annex E. Acceptable Port connection segments are those whose output signal does not intrude within the receiver pulse mask under the test conditions defined in clause 0.

If the Port connection segment is to be a restricted to a single speed connection, it need only be tested under that speed s conditions. A more general Port connection segment shall be tested using the pulse masks pertaining to both the 200 Mb/s and 400 Mb/s speeds.

The input slew rate used shall be no greater than the minimum slew rate shown in Table 5.

The driver test environment shown in 7.1.2 and the associated measurement procedure shall be used when setting the input signals applied at point M2. Once the input signals have been set, the port connection segment shall be connected in place of the driver test load and measuring equipment. The Port Connection Segment test load (see Figure 16) and the measurement procedure shown in 7.1.2.1 shall be used at point M3. The Port Connection Segment test load with scope probes attached shall conform to the characteristic impedance requirements in 7.3 at its connector. The value of each of the two capacitors LC shall be adjusted such that the total capacitance of LC and its associated probe causes the impedance around its time point, measured from its respective LineIn to ground, to fall below 60 ohms for 360 to 375ps. Typically the total capacitance of LC and scope probe will be in the order of 2.5 pF. The values of LR, X and Y in Figure 16 shall be 75 $\Omega \pm 1\%$, 5 cm $\pm$ 5 mm, and 5 mm $\pm$ 1 mm respectively.

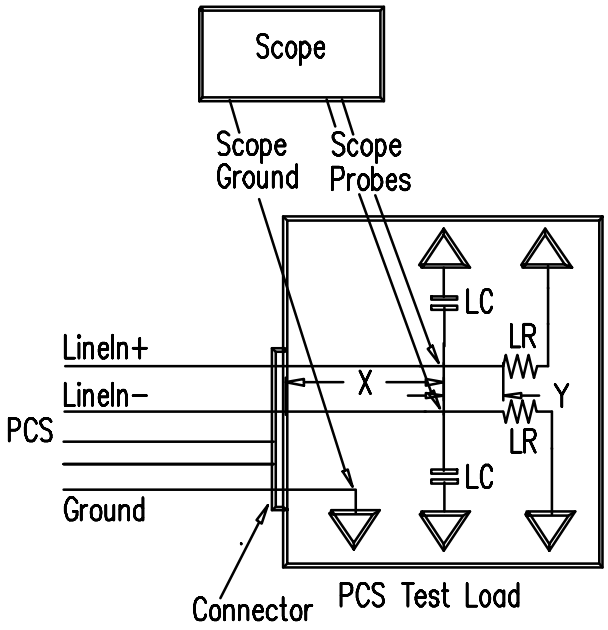


Figure 16 - Port connection segment test load

It is not required to vary the common mode or ground shift levels for the port connection segment tests.

Port connection segments shall be independently tested for each length differing by more than 2 cm or 2.5% of the longer length, whichever is larger. Independent tests shall also be performed for any change in the material, connector, or cable construction. Where the measurement of the physical length is impractical, then the length may be determined using TDR techniques and converted to a length using a conversion factor of 120 ps/cm.

7.5.2 Port connection segment marking

The hardware comprising the Port connection segment should be clearly marked to indicate the speeds for which it meets requirements. Physically inseparable Port Connection Segments (i.e. backplanes) need only be marked once.

7.5.3 Cable assembly

A Cable Assembly provides the simplest form of a port connection.

The term Cable Assembly refers to a cable with connectors, backshells and retention schemes on each end. The cable may consist of media other than extruded insulated wire (e.g., backplanes). The maximum length of a Cable Assembly is not defined as long as its performance requirements are met.

See 8.5.1.6 for external and 8.2.2 for internal cable assembly wiring requirements.

The shield of the bulkhead mounted connector shall be directly connected to the exterior conducting wall that provides the shield function for the enclosure. The effectiveness of this shield connection shall be verified using the test procedures defined in 8.5.4. 360 degree shielding contacts are recommended.

NOTE 4 - An example of a set of electrical parameters that have been found to work for long copper cables with polypropylene dielectrics is provided for reference in Annex J.

Equalization circuits may be used on the signal lines within the cable assemblies. These circuits may increase the length of cable that meets the requirements. All requirements apply for both equalized and non-equalized cable assemblies.

7.5.4 Complex port connection

A Complex port connection is any means of connecting ports other than with a single Cable Assembly.

One form of complex port connection is a series combination of cable assemblies as shown in Figure 17. For example, this may be used when penetrating a shielded enclosure to form a connection between an external and internal Cable Assembly. In this case it is necessary that each individual Cable Assembly be better than the minimum requirements so the series combination meets the requirements.

NOTE 5 - It is the responsibility of the system integrator to work with their suppliers to ensure the Complex Port Connection meets the requirements of this standard.

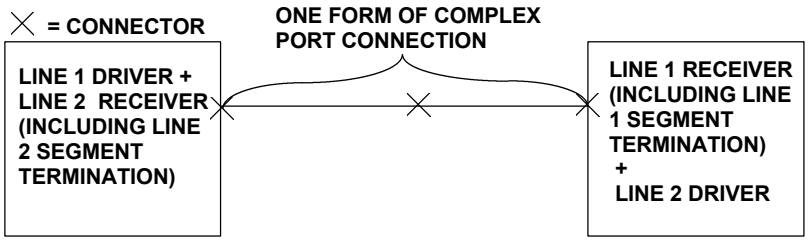


Figure 17 - Complex Port Connection

Port connections implemented with single cable assemblies using passive equalizers are not considered to be complex port connections.

7.5.5 Port connection couplers

It is also possible to construct a complex port connection that consists of active elements such as resiliency circuits and repeaters. The general form of such an element is shown in Figure 18 and entities satisfying the requirements defined in this clause are termed port connection couplers (PCC). Within the PCC boundaries optical or other means of transmitting the signals between the line segment termination side and the line driver side may be used.

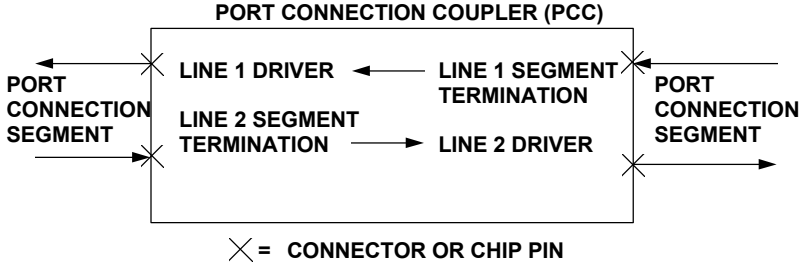


Figure 18 - Port connection coupler

PCCs shall have line drivers that meet all the requirements for SSA port line drivers when worst case compliant SSA receiver signals are presented to the line segment termination side. PCCs are not required to support any character recognition or transport layer functions. They may retime the signals to recover jitter by using local clock references and may amplify signals.

Only receivers capable of reporting bit error rates shall be used as valid M4 points. On the other hand, any connector may be used as a valid M1 driver point.

Elements having the general architecture of PCCs but not meeting the specified driver requirements may have interchangeability problems and port connection segment lengths may need to be reduced. Only the requirements at the port connectors apply if interchangeability at the PCC level is not required.

The maximum round trip delay of a signal through a port connection shall not exceed the ACK time-out (see SSA-TL2). This time includes the propagation time for the media, connectors, PCCs and remote port processing time.

One may use multiple PCCs in the same port connection. Figure 19 shows examples using two and three PCCs.

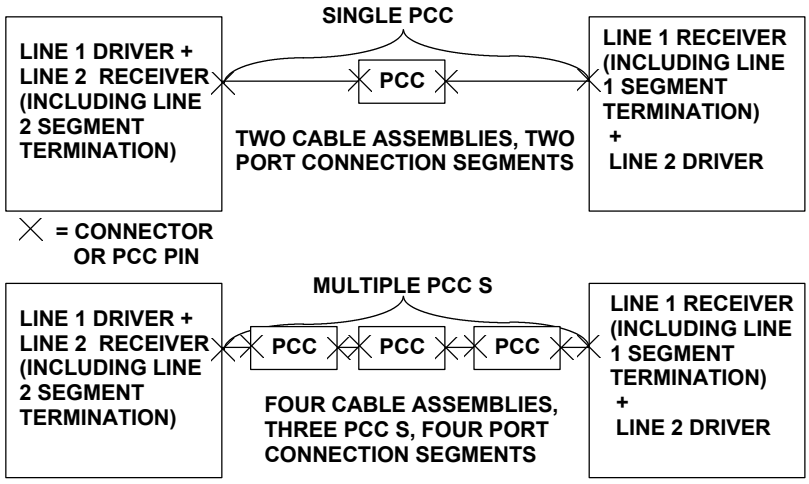


Figure 19 - Complex port connection examples using PCCs

7.5.6 Pulse mask at M2

The input signals for the line test shall be adjusted for amplitude and jitter to match the weakest allowable line driver signal defined in 7.1.

7.5.7 Pulse mask at M3

The output signal for the line test shall remain outside the shaded area and be wholly contained within the V2 and -V2 voltage levels of the line receiver input pulse mask defined in 7.2.4.

7.6 System level noise margin

The requirements in clause 7 leave a full order of magnitude in the link bit error rate for purposes of accommodating noise that may be present during real system operation but not present during the execution of the tests defined in clause 7 (termed system noise). The receiver shall not exceed 10^{-13} bit error rate under the receiver tests but the individual links in the overall SSA system shall not exceed 10^{-12} bit error rate in operation.

Additional margin may be available for systems noise because each of the three major link components (drivers, lines and receivers) have to be independently and simultaneously operating at the extreme limits of their respective requirements to produce the 10^{-13} bit error rate (without system noise).

The requirements for drivers and receivers require that the expected noise from system operation be present during their tests. This includes common mode noise and ground shift noise. The system noise is therefore only noise that exceeds these levels and noise from undefined sources.

8 Interconnections

The electrical connection between two ports consists of the entire electrical path involved. 7.5 addresses the electrical performance requirements for the line segments between the port connectors. 7.1 and 0 govern the electrical performance of the electrical path contained within the ports. The electrical media used to create this path is not defined in this standard. The connectors and their securing schemes are defined to the extent necessary to achieve interoperability between connectors designed and manufactured by different sources.

Some common line media are insulated wires (coaxial, twisted pair, flat), printed circuit board traces and connector pins.

For lines external to node physical frame boundaries (termed external lines) it is generally necessary to provide an electrical shield for the media. This is required to prevent EMI from the electrical activity on the lines and to protect the lines from external interference.

For lines internal to node frame boundaries (termed internal lines) a shield may be needed. The need for a shield for an internal lines depends on the noise present within the node frame and the sensitivity of other elements (including other SSA lines) to radiation and coupling from the electrical activity on the line itself.

The determination of whether a shield is needed for an internal line may be made by applying the tests defined in clause 7.

The physical and electrical requirements of an internal device differs from those of an enclosure resulting in different connectors.

There are two kinds of connector system defined:

a) external shielded with positive retention,
b) internal unshielded with passive retention that mates with either cables or backplanes.

Each of these connector systems contain pins and other features that serve power distribution, grounding and ancillary functions for storage devices as well as providing part of the line. For this reason a complete description of the function of all the pins is provided for the connector systems.

8.1 Internal connectors

The internal device interface allows options to accommodate a wide range of applications in a cost effective manner. These options include a second port that may be configured as either a repeater or a second port (i.e., dual path).

The internal connector is partitioned into three functional parts:

a) port connectors;
b) power connectors;
c) options connectors.

There are three types of connectors defined:

a) a device connector for an SSA node;
b) cable connectors for cable assemblies;
c) a unitized connectors for blind mating backplane printed wiring boards.

The unitized device connectors are designed to mate with cable backplane connectors. This allows a single device physical interface to serve both applications.

Table 11 - Internal connector options

Physical implementation	Port	Power	Options
Device	Device port (6 pin)	Device power (16 pin)	Device options (10 pin)
Cable	Cable port (6 pin)	Cable power (16 pin)	Cable options (10 pin)
Unitized Device	All three functions with two port connections - 38 pins in four bays (accepts all three cable function options and mates with unitized backplane connector).		
Unitized Backplane	All three functions with two port connections - 38 pins in four bays (mates with unitized device connector only).		

The pin assignments for internal connectors are shown in 8.2, 8.3 and 8.4. Note that devices with different port, option and power requirements only need to implement a subset of these pins.

All connector contacts shall be rated to carry 1.5 A with a maximum temperature rise of 20 degrees C.

Figure 20 through Figure 29 describe the unitized backplane and cable connectors. The unitized backplane connector is segmented to form four separate bays and is intended for blind mate applications when used with the unitized device connector. Each bay has flexing contacts recessed within the housing for protection against damage. The cable connectors are intended to mate with the individual bays on the unitized device connector

Figure 30 and Figure 31 describe the unitized device connector that is segmented to form four separate bays.

Figure 33 through Figure 37 define the device connector details. Each has solid, non-flexing contacts recessed within the housing for protection against damage. Defined contacts in each connector are extended toward the mating face to provide first-make, last-break capability. Each connector also contains a number of recessed detents to provide detent retention.

Figure 20 and Figure 30 describe the outer plastic profile for the unitized versions, that prevents mechanical damage to the flexing contact members. This assures adequate lead-in for the device connectors, and provides proper contact registration with the contact blades in the unitized connector. Figure 26 and Figure 37 illustrate the contact used in the connectors. Each bay in the plastic shell also provides detents that mate with the recesses on each housing as defined in Figure 36.

Figure 27 shows the necessary contact information to assure an adequate contact wipe distance. It also describes the force to be exerted by the plug contact at the point Fn as the Hertz normal force and the plug contact as the Hertz mating surface. Interface performance criteria are found in Annex B.

The mating interface is a leaf style design. The cable and backplane connector contacts are compliant, with a coined contact area. The device connector contact is fixed.

8.1.1 Cable connectors

The mating features and the face view dimensions of the cable and backplane connectors are shown in Figure 28 and Figure 29. These assure the side-to-side stacking and intermateability of the cable and backplane connectors with the corresponding device connectors.

8.1.2 Cable connector termination

The termination of discrete stranded wire or ribbon cable to the cable connectors may be varied to suit the manufacturing process needs of the cable assembler. Since the backside termination does not affect the intermateability of the connector/Cable Assembly, any termination technique may be used, provided it meets the performance requirements in 7.5 and the overall dimensions given in 8.1.

For reference, the following acceptable methods are listed:

a) Crimp;
b) Insulation Displacement (IDT);
c) Insulation Piercing;
d) Welding;
e) Soldering.

8.1.3 Cable media

The cable media may be of any form that allows the performance requirements in 7.5 for the overall Cable Assembly. In general it is advisable to used balanced media where the Line+ and the Line- have the same surroundings and follow the same physical path. Flat ribbon cable is notable for its unbalanced features in this application but may nevertheless be used if the performance criteria are met.

8.1.4 Contact finish on mating surfaces of connector contacts

The electroplated finish on the mating surfaces shall assure the compatibility of connectors from different sources. The following examples are compatible electroplatings and may be used on mating surfaces of contacts:

a) 0,76 μm (30 μin.), minimum, Gold, over 1,27 μm (50 μin.), minimum, Nickel;

b) 0,05 μm (2 μin.), minimum, 0,127μm (5 μin), maximum, Gold, over 0,76 μm (30 μin.) minimum, Palladium, over 1,27 μm (50 μin.), minimum, Nickel;

c) 0,05 μm (2 μin.), minimum, 0,127 μm (5μin.), maximum, Gold, over 0,76 μm (30μin.) minimum, Palladium-Nickel Alloy (80% Pd-20% Ni), over 1,27 μm (50μin.), minimum Nickel.

Selective plating on contacts is acceptable. In that case, one of the above electroplatings shall completely cover the area of contact, including the entire contact wipe area. A copper strike is acceptable, under the nickel electroplate. A palladium strike is acceptable, over the nickel electroplate.

8.1.4.1 Internal unitized backplane connector

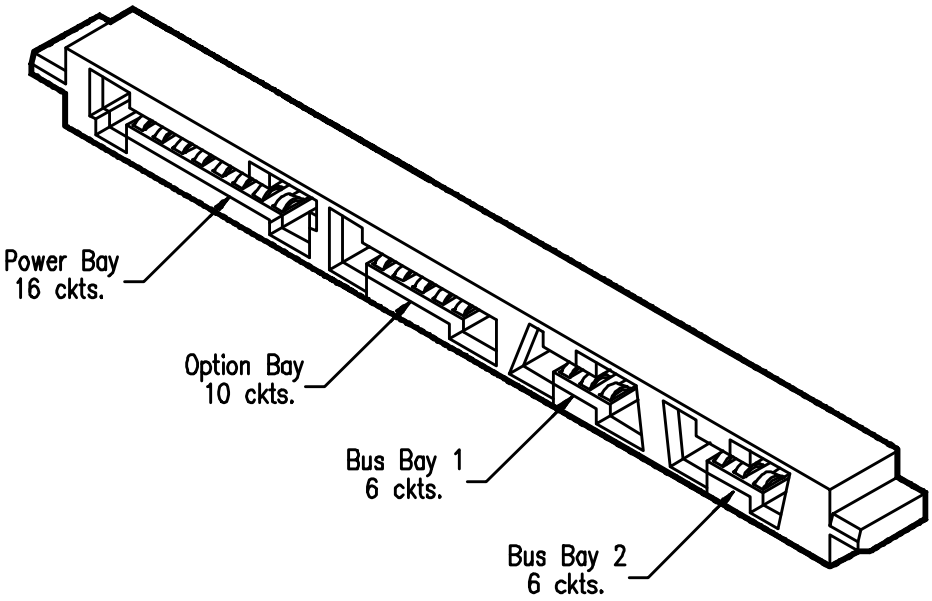


Figure 20 - Internal unitized backplane connector overview

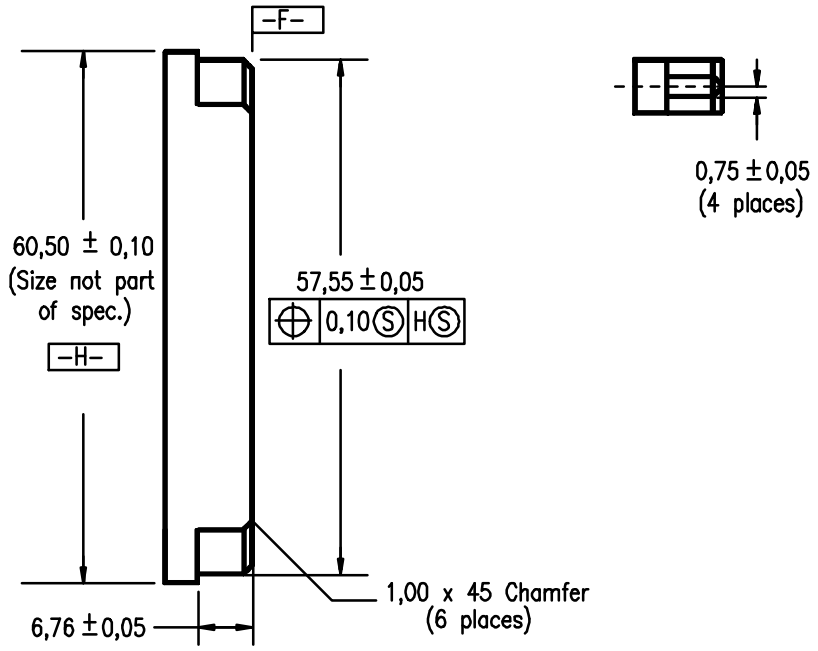


Figure 21 - Internal unitized backplane connector detail (side view)

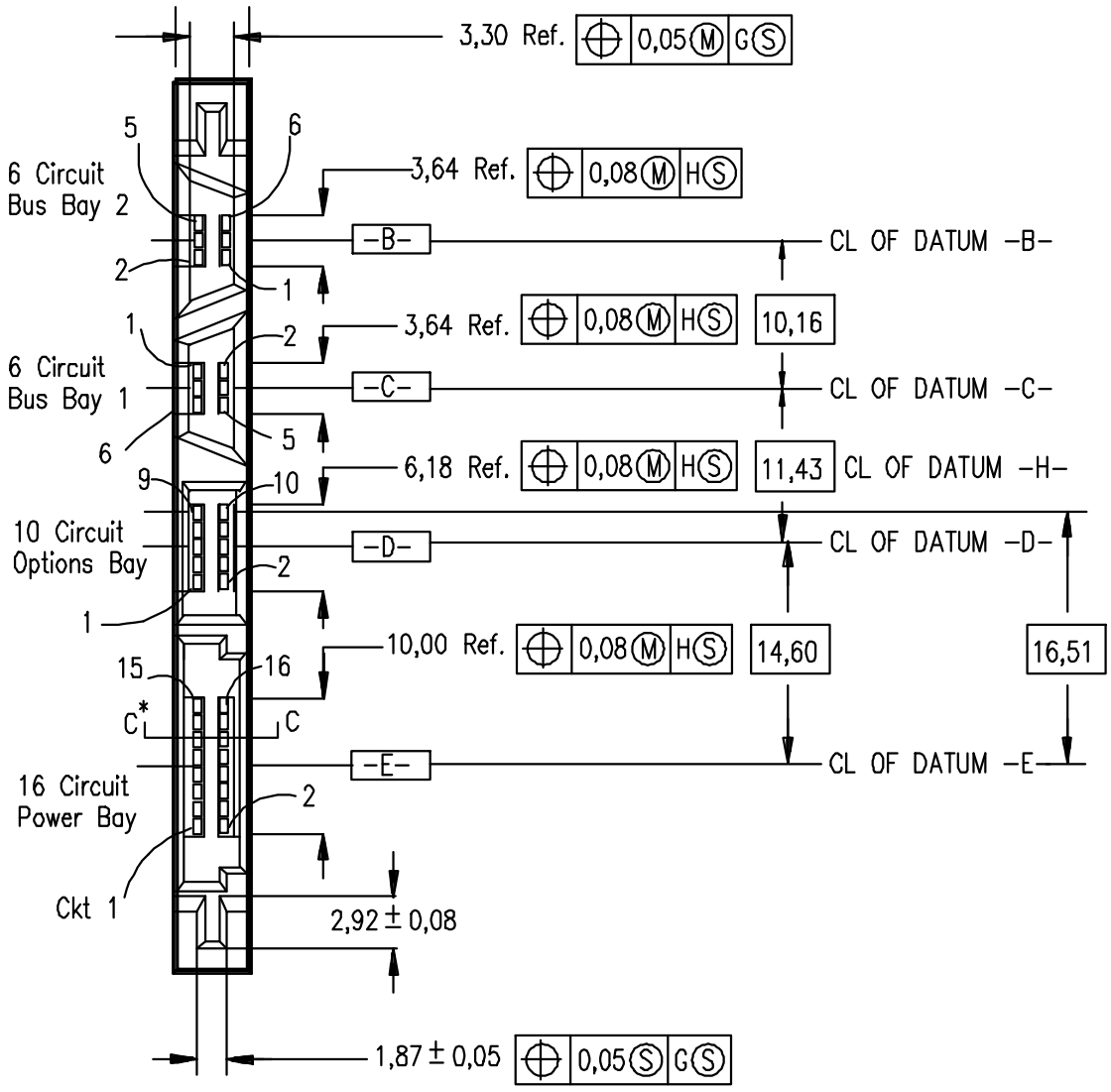


Figure 22 - Internal unitized backplane connector detail (end view)

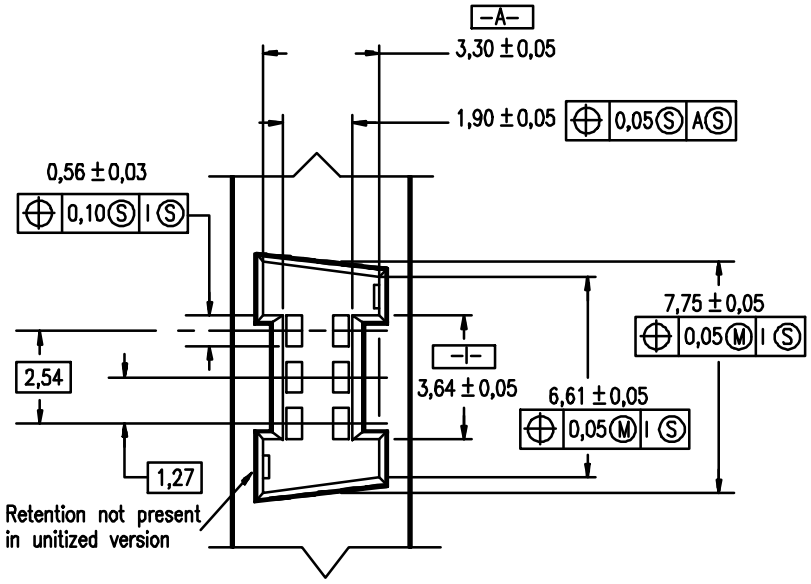


Figure 23 - Internal cable and backplane port connector detail

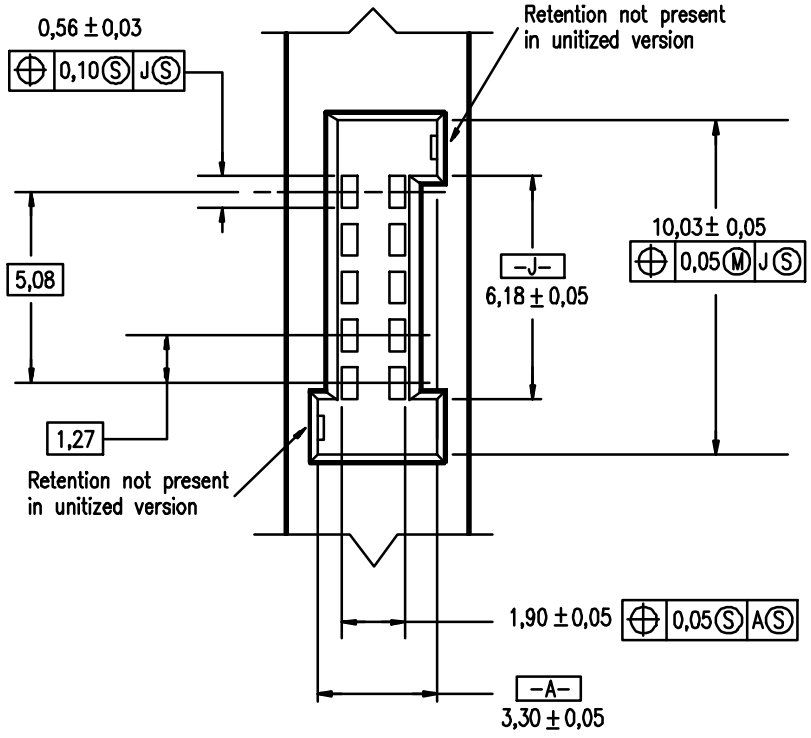


Figure 24 - Internal cable and backplane option connector detail

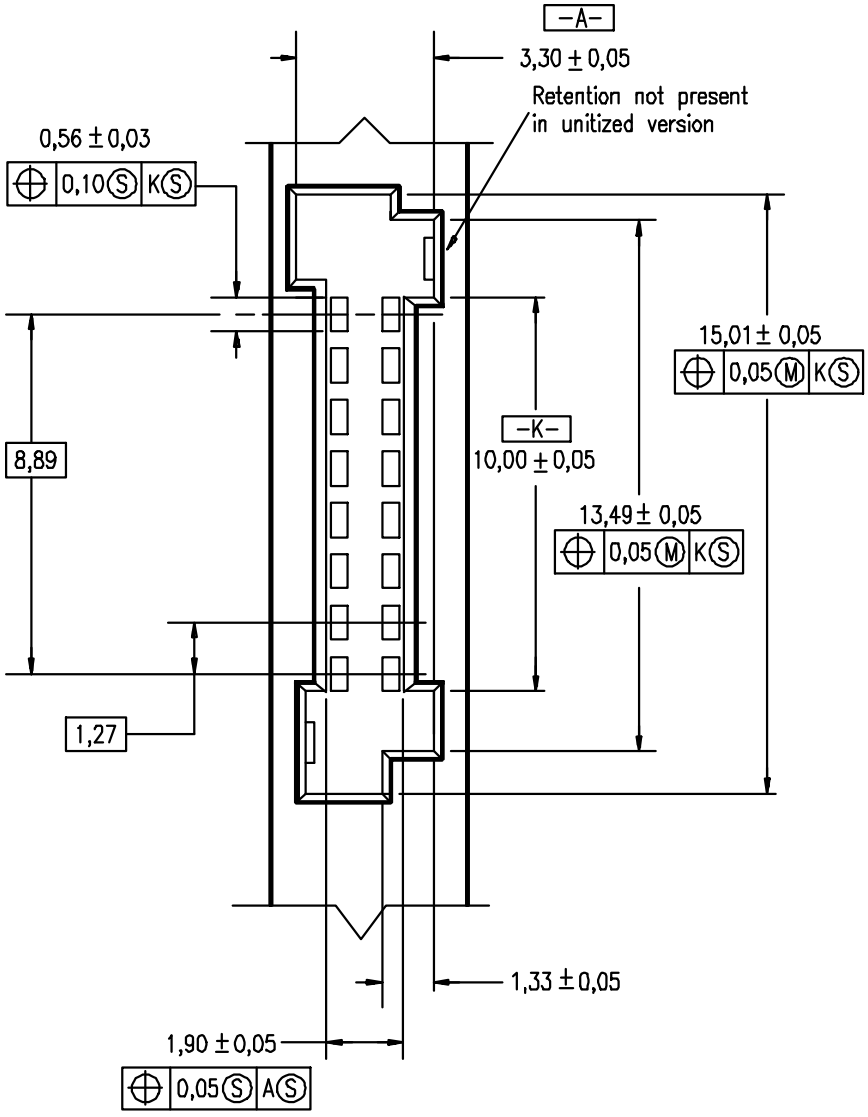


Figure 25 - Internal cable and backplane power connector detail

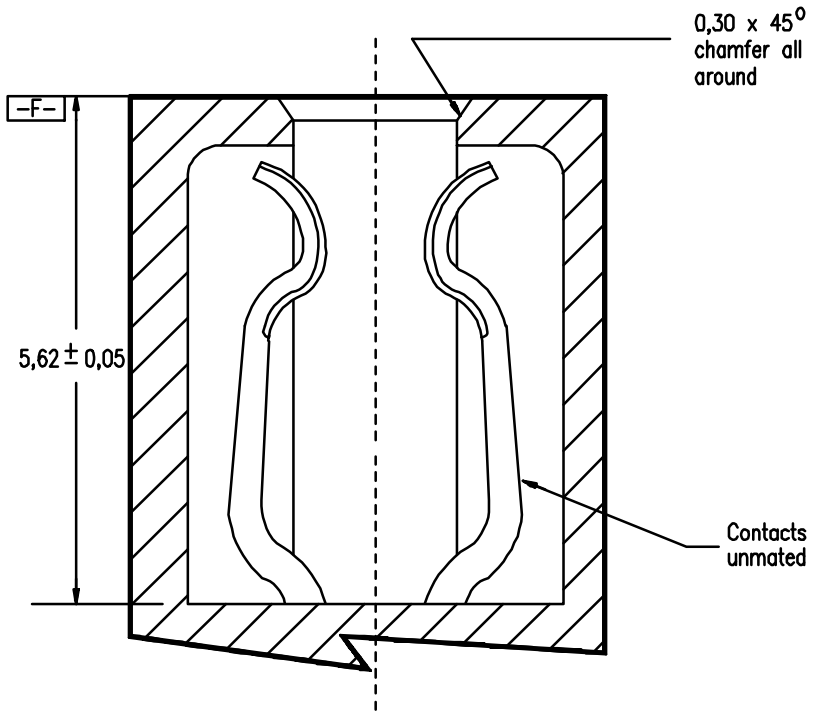


Figure 26 - Internal cable and backplane connector contact detail

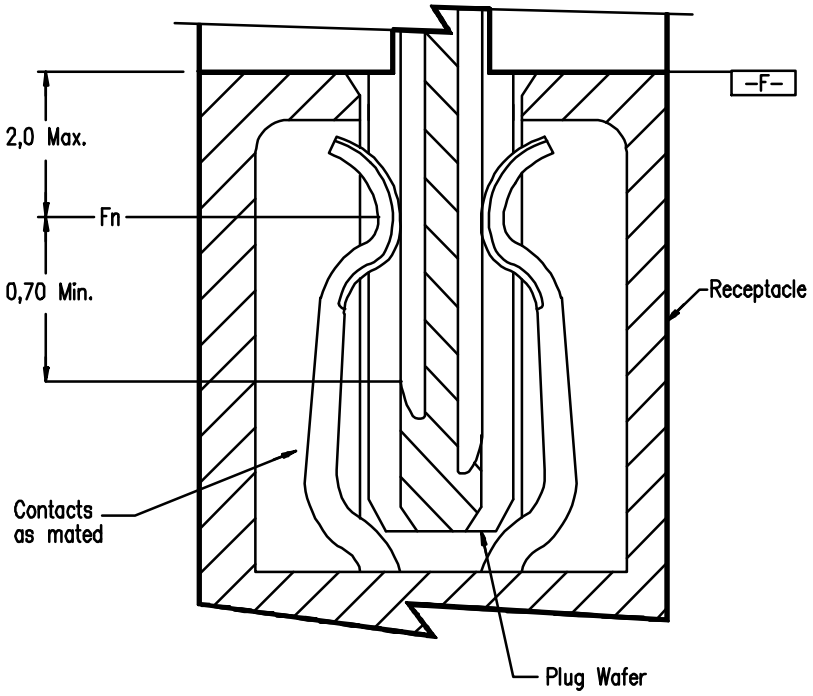


Figure 27 - Internal cable and backplane connector contact wipe detail

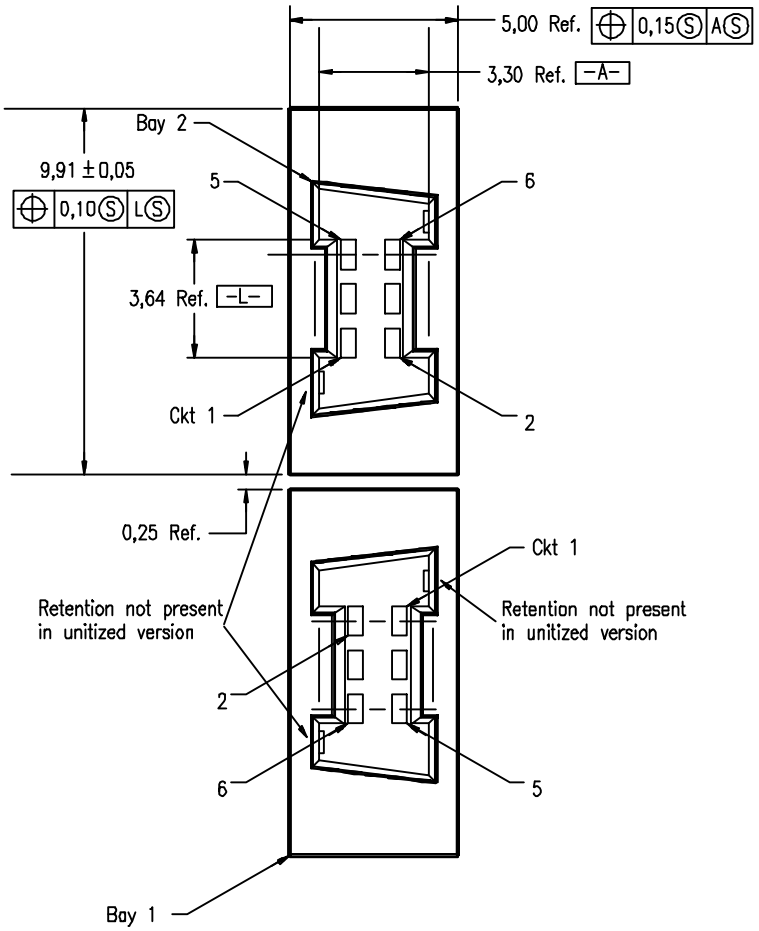


Figure 28 - Internal cable and backplane port connector detail (2 ports shown)

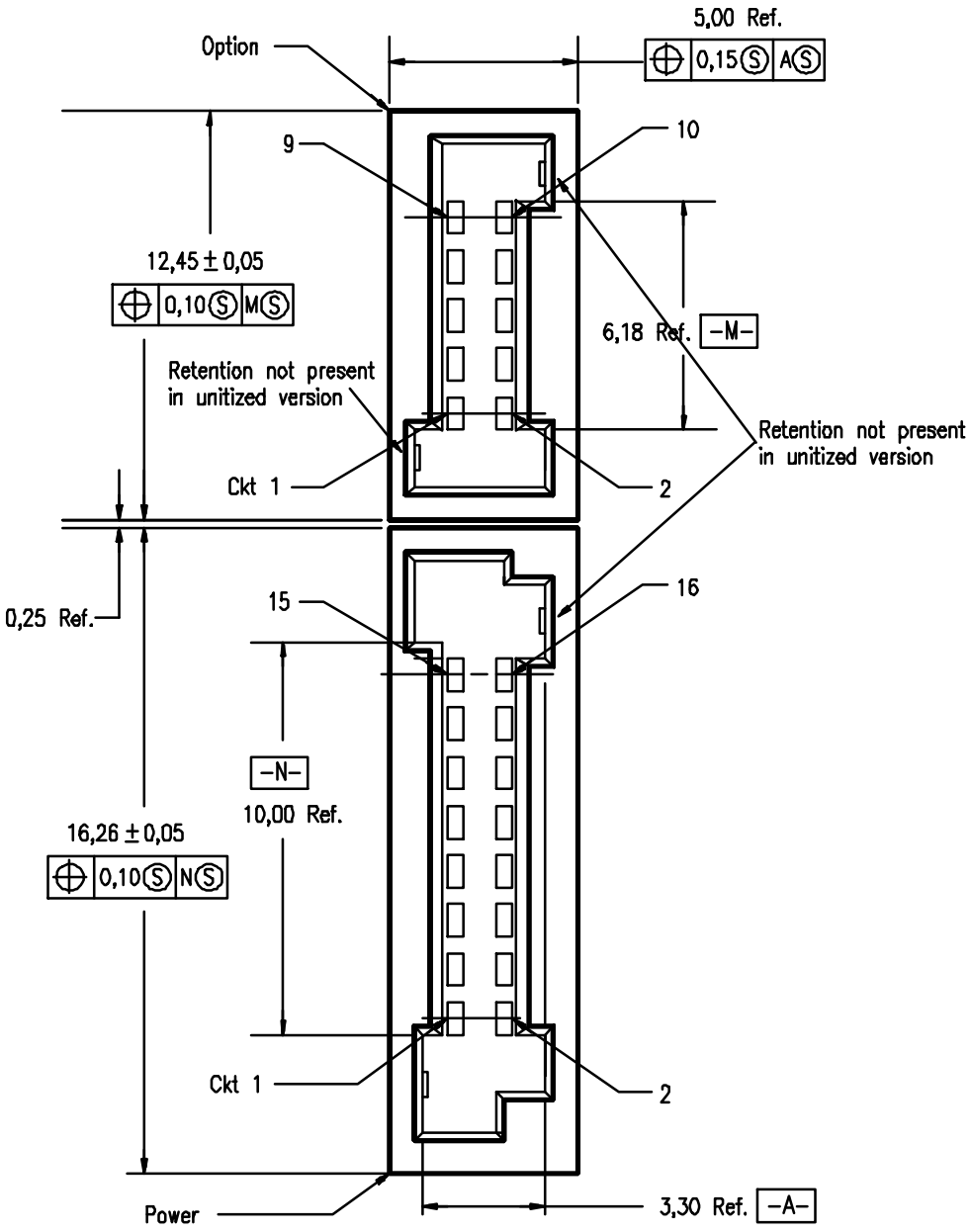


Figure 29 - Internal cable and backplane option and power connector detail

8.1.4.2 Internal unitized device connector

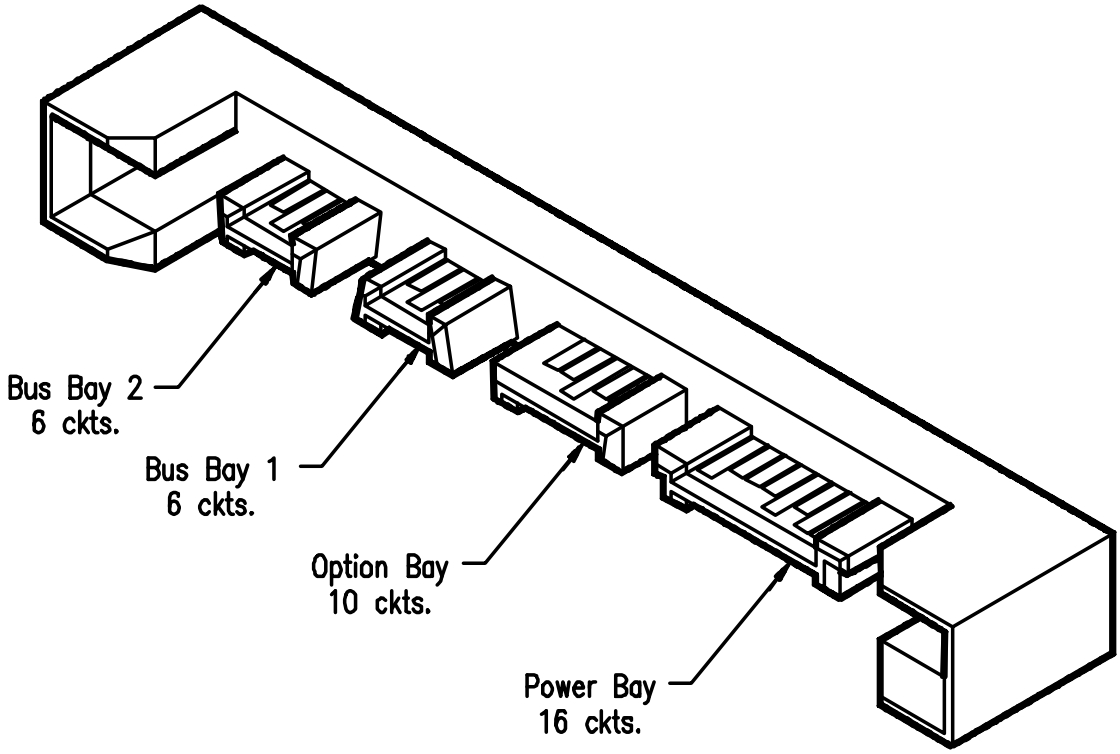


Figure 30 - Internal unitized device connector overview

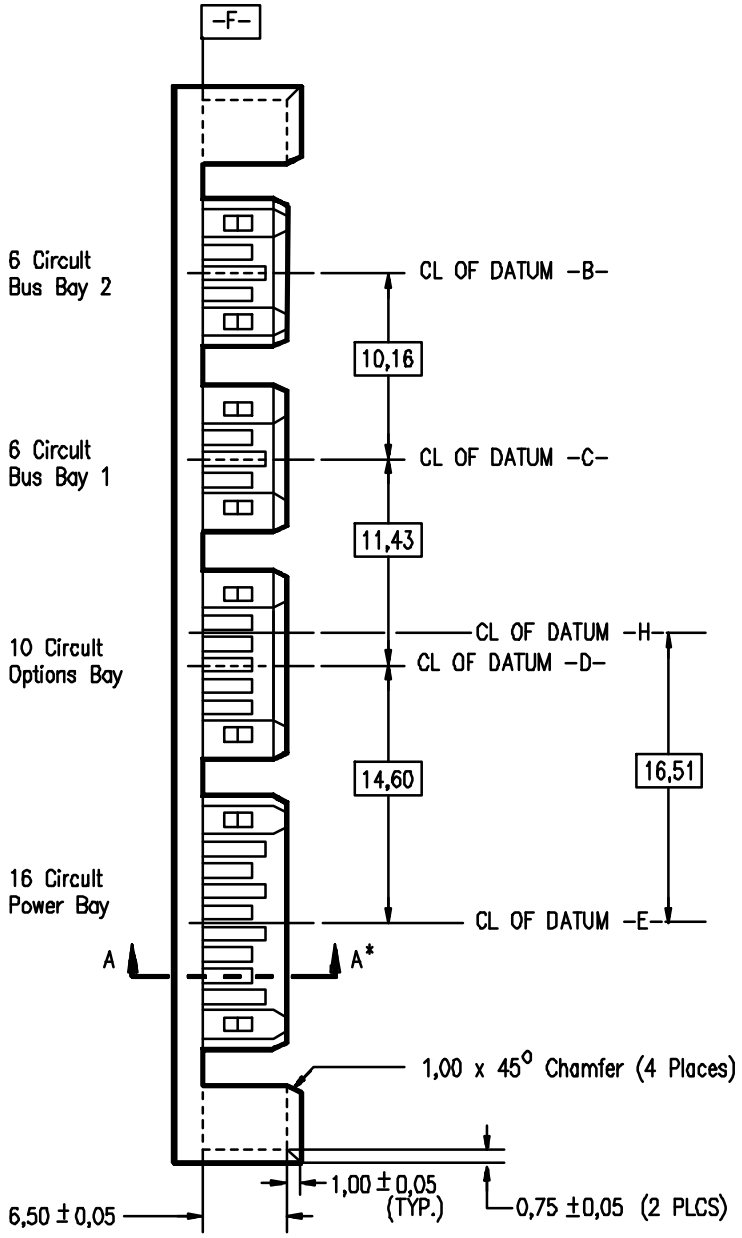


Figure 31 - Internal unitized device connector detail (top view)

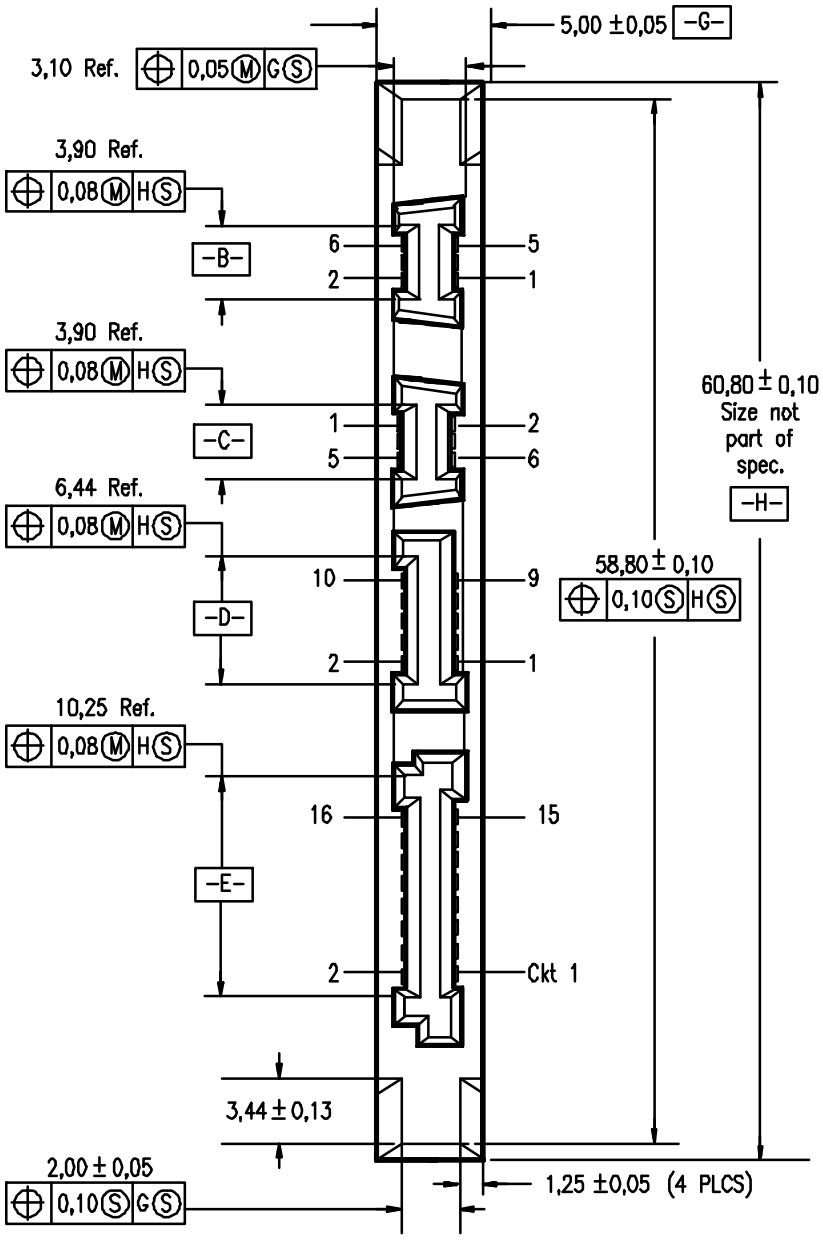

5,00 ±0,05 -G-
3,10 Ref.
0,05 M G S
3,90 Ref.
0,08 M H S
-B-
6
5
2
1
3,90 Ref.
0,08 M H S
-C-
1
2
5
6
6,44 Ref.
0,08 M H S
-D-
10
9
2
1
10,25 Ref.
0,08 M H S
-E-
16
15
2
Ckt 1
60,80 ± 0,10
Size not
part of
spec.
-H-
58,80 ± 0,10
0,10 S H S
3,44 ± 0,13
2,00 ± 0,05
0,10 S G S
1,25 ±0,05 (4 PLCS)

Figure 32 - Internal unitized device connector detail (end view)

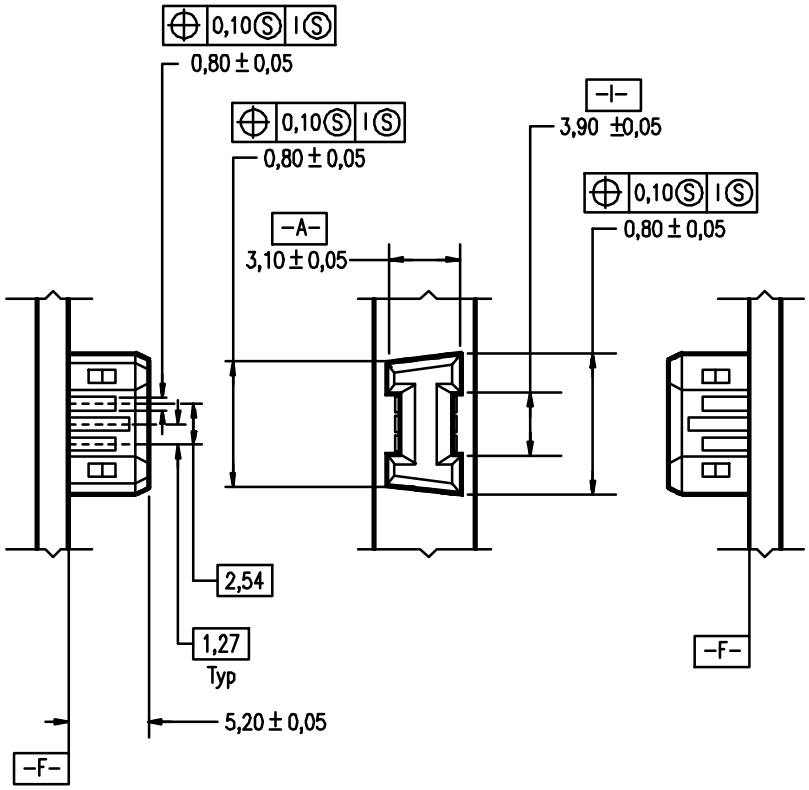


Figure 33 - Internal device port connector detail

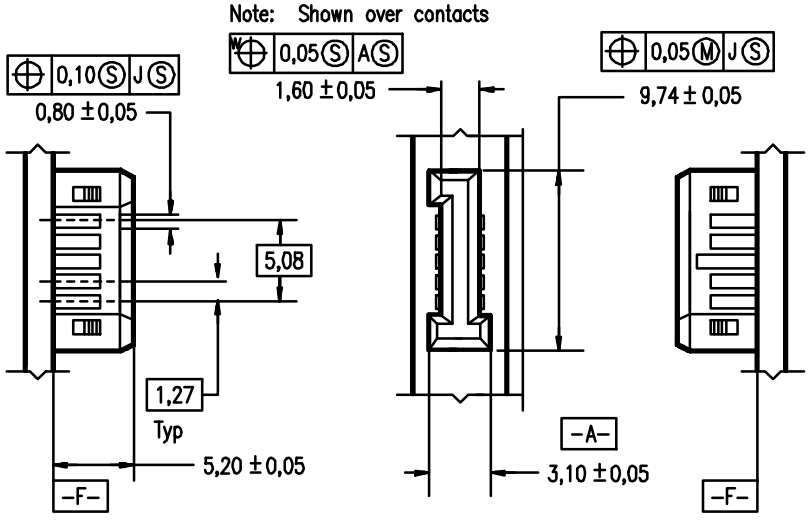


Figure 34 - Internal device options connector detail

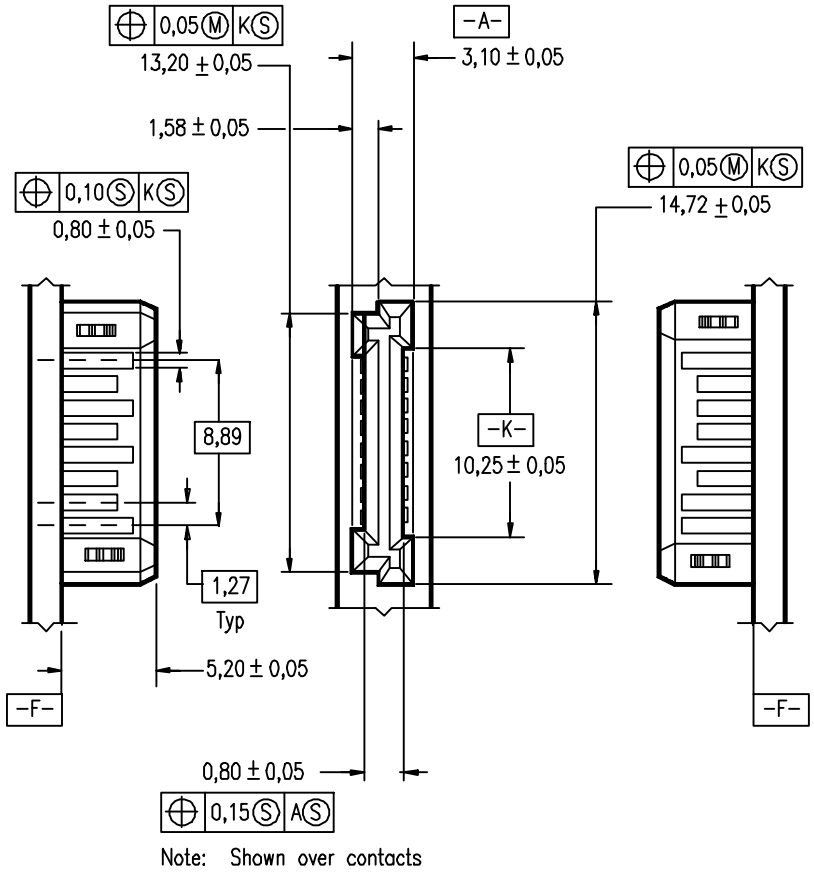


Figure 35 - Internal device power connector detail

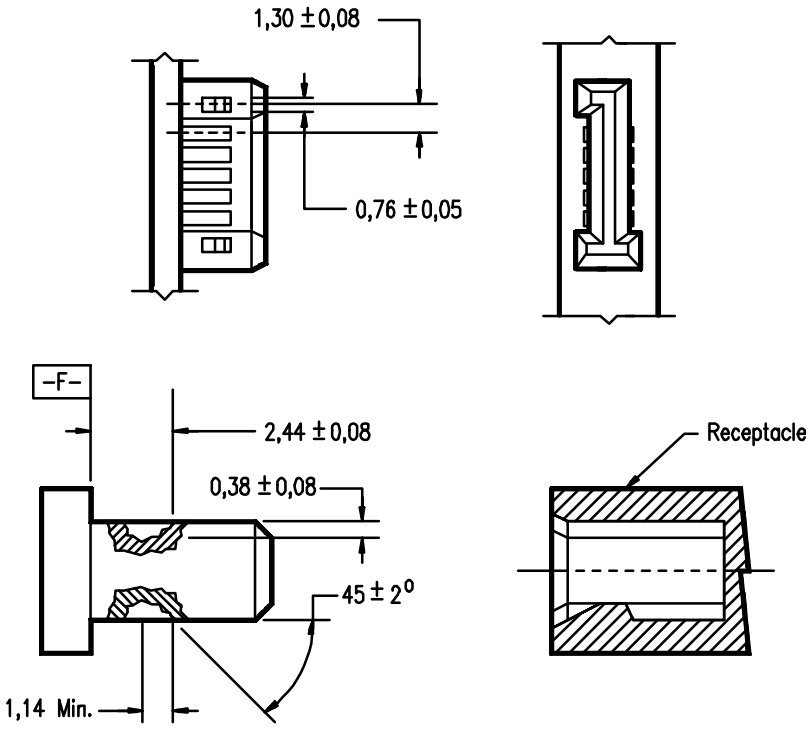


Figure 36 - Internal device connector retention detail

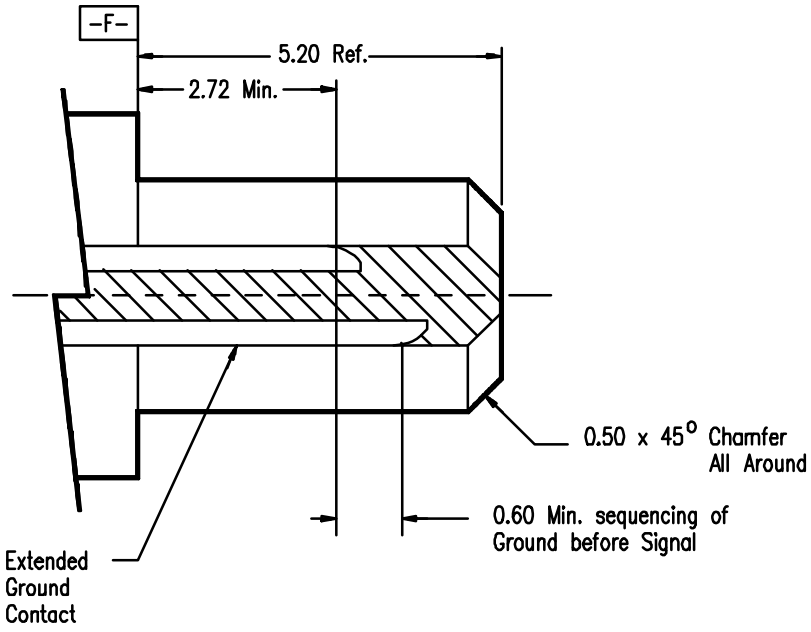


Figure 37 - Internal device connector pin sequencing detail

8.2 Internal port connections

An internal port cable contains 4, 5 or 6 conductors. The required conductors are the LineOut and LineIn signals. The construction is implementation-dependent, e.g. twisted-pairs, twinax, flexible flat cable.

The internal port cable may require shielding in some implementations to meet the requirements for an SSA node the use of shielding on internal cables is optional.

If shielding is used, the shield shall be connected to pin 3 in the internal device port bay receptacle, this in turn shall be connected to chassis/power ground in the device. Pin 4 in the internal device port bay receptacle shall be logic ground and shall not be connected to the shield in the internal Cable Assembly. If there is no chassis/power ground available in the device, the shield pin (pin 3) shall be connected to the logic ground on the device side of the connector.

In order to allow for the possibility that a 6-line unshielded connection (see 8.2.2.3) may be used in the cable wiring, special care is required in placing the logic ground connection to pin 4 in the device. The 6-line connection used with flat, mass terminated cable forces the chassis/power ground on one end of the Cable Assembly to be connected to the logic ground on the other end and vice versa. The device shall place the pin 4 logic ground connection as close as possible to the nearest chassis/power ground point. This establishes a single ground point within the device as much as possible while minimizing the noise in the logic ground in the device. Since the 6-line connection does not allow a shield connection to any internal port device connector pin, shield noise is not directly coupled to logic ground.

The preferred implementation is the 5-line connection (see 8.2.2.2) using a balanced shielded cable media. Since balanced media require special attention for Cable Assembly termination the logic ground connection remaining on the same pin number on both ends is a very minor inconvenience.

If multiple termination to the same connector pin is possible then additional logic ground lines may be used for purposes of achieving balance in the cable media.

8.2.1 Internal device port connector pinouts

The pinout for the signals on the device side of the connector is listed in Table 12. Device refers to disks, controllers or other entities acting as an SSA node.

Table 12 - Pinouts for internal port device connectors

Pin	Port device plug & cable receptacle
1	LineOut+
2	LineOut-
3	Chassis/power ground
4	Logic ground
5	LineIn-
6	LineIn+

8.2.2 Internal cable and backplane port pinouts

The internal cable port connections differ depending on the construction of the cable media. When backplanes are used there is no need to consider a shield so the any of the cable pinout options may be used. Backplanes also offer the advantage that not maintaining physical pin order does not imply a cost premium. Cables offer the advantage of easy system level routabilty and easy user flexibility for reconfigurations.

8.2.2.1 Internal cable and backplane port 4-line connections

When using cable media with four lines plus an optional shield the pinouts in Table 13 shall be used. The shield is connected to the same pin number on both sides in contrast to the lines that are connected to different pin numbers on both sides. This requires careful attention in the Cable Assembly.

Table 13 - Pinout for 4-line Internal port device connections

Conductor	Receptacle 1		Receptacle 1	
	Pin	Signal name	Pin	Signal name
1	1	LineOut+	6	LineIn+
2	2	LineOut-	5	LineIn-
Shield[1] (optional)	3	Chassis/power ground	3	Chassis/power ground
No connection	4	Logic ground	4	Logic Ground
3	5	LineIn-	2	LineOut-
4	6	LineIn+	1	LineOut+
NOTE [1] - Both ends of the shield shall be connected in the Cable Assembly				

8.2.2.2 Internal port 5-line connections

When using cable media with 5-lines plus an optional shield the pinouts in Table 14 shall be used. Note that the shield and the logic ground are connected to the same pin number on both sides in contrast to the lines that are connected to different pin numbers on both sides. This requires careful attention in the Cable Assembly.

Table 14 - Pinout for 5-line internal port device connections

Conductor	Receptacle 1		Receptacle 1	
	Pin	Signal name	Pin	Signal name
1	1	LineOut+	6	LineIn+
2	2	LineOut-	5	LineIn-
Shield[1] (optional)	3	Chassis/power ground	3	Chassis/power ground
3	4	Logic ground	4	Logic Ground
4	5	LineIn-	2	LineOut-
5	6	LineIn+	1	LineOut+
NOTE [1] - Both ends of the shield shall be connected in the Cable Assembly				

8.2.2.3 Internal port 6-line connections

When using cable media with 6-lines the pinouts in Table 15 shall be used. If a shield is used it shall not be connected to any pins defined 8.2. This construction connects the logic ground to the power ground through the Cable Assembly or backplane and is not desirable.

Table 15 - Pinout for 6-line internal port device connections

Conductor	Receptacle 1		Receptacle 1	
	Pin	Signal name	Pin	Signal name
1	1	LineOut+	6	LineIn+
2	2	LineOut-	5	LineIn-
3	3	Chassis/power ground	3	Logic ground
4	4	Logic ground	4	Chassis/power ground
5	5	LineIn-	2	LineOut-
6	6	LineIn+	1	LineOut+

NOTE 6 - A 6-line internal port cable may be built with mass terminated ribbon cable without cuts.

8.3 Internal options bay connections

8.3.1 Electrical characteristics

All option bay signals are TTL level compatible. In addition, four signals are capable of sinking sufficient current to drive LEDs. All signals are negative active.

Table 16 - TTL input pin parameters

Characteristic	Minimum	Maximum
Input Leakage	-10 µA	+10 µA
Input High	+2,0 V	+5,5 V
Input Low	-0,5 V	+0,8 V

Table 17 - TTL output pin parameters

Characteristic	Minimum	Maximum	Conditions
Tri-state Leakage	-10 µA	+10 µA	-0,5 V to 5,5 V
Output High	2,4 V	5,5 V	Output current = 800 uA
Output Low	0,0 V	0,4 V	Output current = 4 mA

The LED capable outputs are current limited open collector outputs that have an LED anode connected directly to 5 V with the LED cathode connected directly to the LED capable output pin. The LED capable output shall be capable of indefinitely sinking the current produced when the pin is shorted directly to 5,5 V and limiting current to no more than 40 mA when on.

NOTE 7 - The requirements may be met with an open collector that is capable of indefinitely sinking 37 mA with a 150 Ω current limiting resistor. However, the normal current draw with a 150 Ω resistor is 28 mA (5,0 V - 0,7 V LED drop divided by 150 Ω).

8.3.2 Options connector pinouts

Table 18 - Options connector pinouts

Pin #	Name	Function
1	Manufacturing Test Mode	Input
2	Auto Start	Input
3	Sync	Input / output
4	Write inhibit	Input
5	Ground(long)	
6	Device Activity	LED capable output
7	+5 V	
8	Device Fault	LED capable output
9	Programmable 1	Input /LED capable output
10	Programmable 2	Input /LED capable output

Manufacturing Test Mode is a low active input pin, that when active (pulled below 0,8 V) makes pins 2, 3, 4, 6, 8, 9 and 10 available to be redefined. Pins 5 and 7 shall remain Ground and +5 V respectively. This pin allows a manufacturing tester to redefine the option pins to whatever functions it desires, while allowing the function of the pins in the shipped product to return to the standard definitions.

Auto Start is a low active input pin, that when active (pulled below 0,8 V) causes the device to become ready for media access after power is applied. When inactive (pulled above 2,0 V) the signal is to be sampled by the device at power on or reset conditions. Media access is controlled by vendor specific means.

Sync is a pin is used to transmit / receive a sync signal. The width, period, and tolerance of the negative active Sync pulse is vendor specific, and thus synchronization across different manufacturers or even different product lines of the same manufacturer is not guaranteed.

Write inhibit is a low active input pin, that when active (pulled below 0,8 V) inhibits writing to user data area. Write inhibit is sampled at power on and reset.

Ground shall be capable of handling 1,0 A of current through this ground pin. This pin is longer than any others in the option block to allow for the ground to mate first.

Device Activity is a low active LED output that activates when the device is active.

+5 V shall source 1,0 A of current at +5 V ± 10%. The maximum source current is 1,0 A at V= 0.

Device Fault is an active low LED output that activates when the device is in an fault condition.

Programmable 1 shall be capable of either being an input or an LED capable output. The function of this pin is controlled by the implementer.

Programmable 2 shall be capable of either being an input or an LED capable output. The function of this pin is controlled by the implementer.

8.4 Internal device power connections

8.4.1 Electrical characteristics

No pin shall exceed 2,25 A peak, 1,5 A continuous.

When a discharged device is hot plugged into a power distribution system, the capacitance in the decoupling capacitors on the printed circuit board causes significant current surges while the capacitance is charging. This current spike may cause arcing and damage the connector pads, as well as cause a voltage drop in the power distribution system that may affect other devices using the system for power. To help this problem, pins 1, 2 and 16 have a resistor or other circuitry in series between the power source and the device connector (not on the device). Additional current limiting circuitry may also be on the device. This allows for a more controlled current draw as the device is being hot plugged. These pins are longer to allow them to mate prior to the other voltage pins. It is up to the subsystem implementer to determine the proper circuitry to add to these lines to meet the current draw limitations of the connector.

8.4.2 Power connector pinouts

The following shall apply to the internal device power connector:

Table 19 - Power connector pinouts

Pin #	Name	FUNCTION
1	+12 V charge (long)	Pre charge for the +12 V system input
2	+5 V charge (long)	Pre charge for the +5 V system input
3	Ground (long)	
4	+12 V	Input
5	+12 V	Input
6	+12 V	Input
7	Ground (long)	
8	Ground (long)	
9	+5 V	Input
10	+5 V	Input
11	Power Fail	TTL input
12	Ground (long)	
13	+3,3 V	Input
14	+3,3 V	Input
15	Ground (long)	
16	+3,3 V charge (long)	Pre charge for the +3,3 V system

NOTE 8 - The +3,3 V charge function has been added using a pin that was formerly used for ground. This change allows the same connector to be used but requires this pin to be disconnected in products using earlier requirements to prevent 3,3 V shorts in systems that use a 3,3 V supply.

Power Fail shall become negative active at least 10 ms prior to power dropping below the 10% tolerance to allow the device a reasonable chance of completing a write operation. Power fail shall stay active low after power has failed to keep the devices in a standby mode as long as the logic is capable of driving the power fail

pin. When in this standby mode, devices shall reject new SMS commands (see SSA-TL2). Should Power Fail be deasserted after assertion, devices shall perform an internal reset (see SSA-TL2).

8.5 External connections

Two different external connector styles are supported, Micro-miniature D, and HSSDC (High Speed Serial Data Connector).

No pin shall exceed 2,25 A peak, 1,5 A continuous.

8.5.1 Micro-miniature D external connector

8.5.1.1 Micro-miniature D shielding and retention schemes

The external connectors are fully shielded for protection against RFI/EMI. They are 9-way micro-miniature D connectors equipped with positive retention schemes:

a) External node connections shall provide a separate shielded device connector for each. The connector shield shall be grounded to the node enclosure in a manner that allows the connector system to satisfy the requirements in 8.5.4. The external shielded device connector has pin contacts.

b) The external Cable Assembly shall be terminated with a shielded cable connector having a metallic shield and a backshell that connects the connector shield to the cable shield in a manner that allows the mated connector system to satisfy the requirements in 8.5.4. The shielded cable connector has socket contacts.

c) A shielded device connector shall be capable of mating with either a jack screw, push/pull detent, or a slide latch jack post. The selection of the scheme actually used is made in the Cable Assembly backshell design

Shield contact between the device and cable connectors is accomplished by three raised lines on the device connector (two top, one bottom).

The external connectors allow any of three different retentions schemes to be used detent, jack screws, and slide latch jackpost. The device connector supports all three. The cable connector implements only one retention scheme and determines what is actually used. If jack screws are used they shall be capable of withstanding 5 inch-pounds of torque and a M1,6 thread shall be used.

The details of the shielded device connector mating interface are shown in Figure 38, the shielded cable in Figure 39.

Retention forces shall be defined as forces on the cable media in a direction perpendicular to the plane of the enclosure wall that is securing the shielded device connector. Jackscrew or slide latch retention shall result in mechanical failure of the Cable Assembly before a failure of the retention itself. For jackscrew or slide latch retention schemes the Cable Assembly shall withstand at least 100 N axial force without mechanical or functional damage. For push-pull retention schemes the maximum and minimum axial forces are 80 N and 45 N respectively. If no positive retention is used the connector shall demate upon applying an axial force of 25 N or more.

8.5.1.2 Micro-miniature D cable connector termination

Any termination technique may be used that allows the final product to meet the performance and dimensional requirements.

8.5.1.3 Micro-miniature D contact finish on mating surfaces of connector contacts

The electroplated finish on the mating surfaces shall ensure the compatibility of connectors from different sources. The following examples are compatible electroplatings and may be used on mating surfaces of contacts:

a) 0,76 μm (30 μin) minimum gold over 1,27 μm (50 μin) minimum nickel;

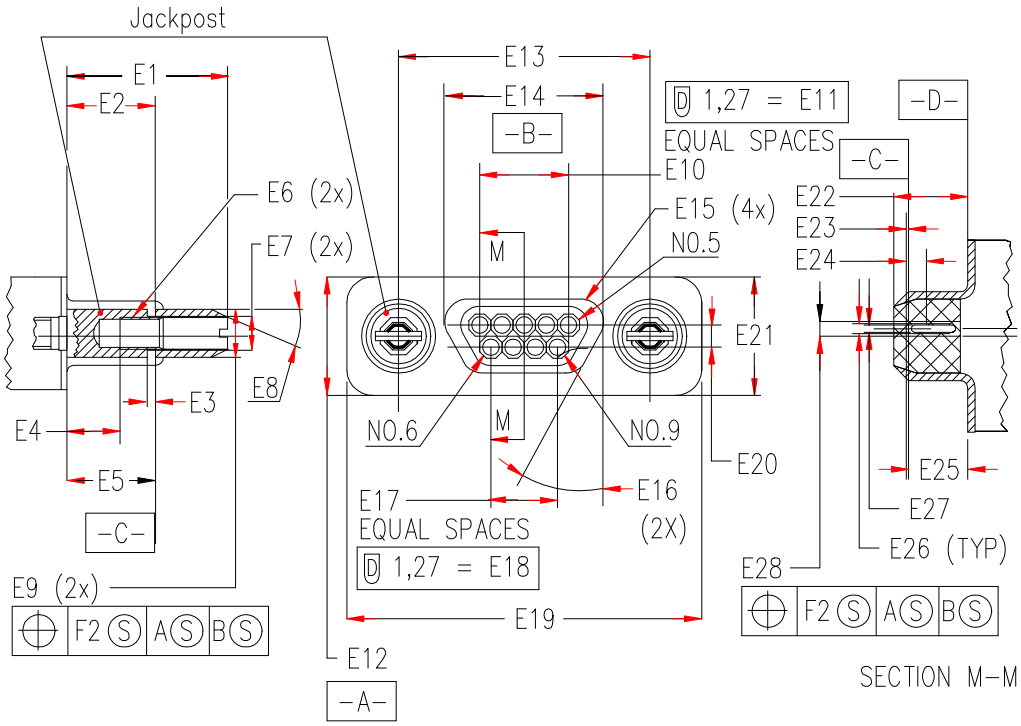
b) 0,05-0,127 μm (2-5 μin) gold over 0,76 μm (30 μin) minimum palladium over 1,27 μm (50 μin) minimum nickel;

c) 0,05-0,127 µm (2-5 µin) gold over 0,76 µm (30 µin) minimum palladium nickel alloy (80%Pd-20%Ni), over 1,27 µm (50 µin) minimum nickel;

d) or 0,1 µm (4 µin) minimum gold over 1,27 µm (30 µin) minimum palladium nickel alloy(80%Pd/20%Ni) over 0,5 µm (20 µin) minimum nickel.

8.5.1.4 Micro-miniature D dimensional requirements

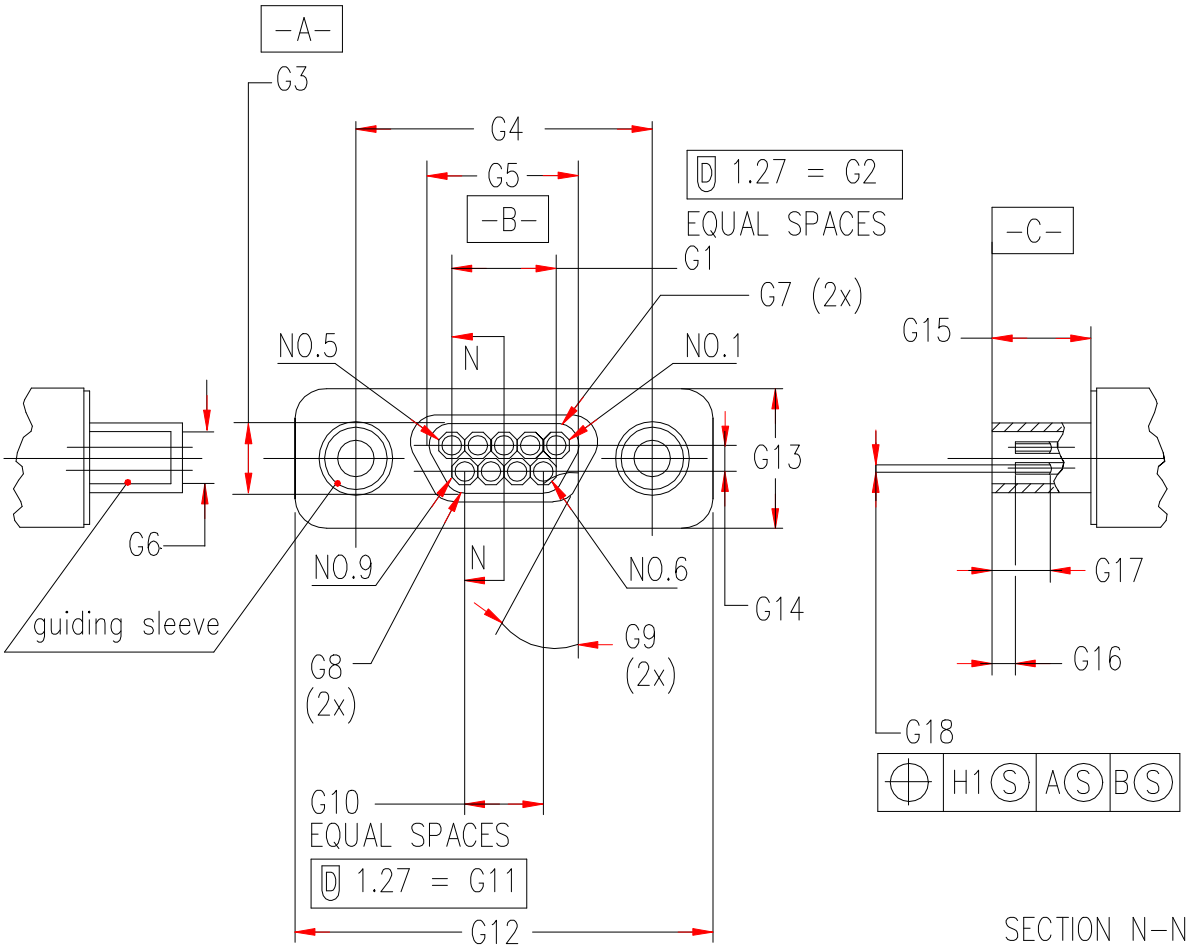
The external connectors shall be designed to meet the dimensional requirements defined in Figure 38 and Figure 39. These requirements are defined in order to ensure intermateability among different manufacturers.



LABEL	DIMENSION	TOLERANCE	VALUE
E1	8,0 MAX	F1	0,2
E2	4,1 ± 0,2	F2	0,2
E3	0,4 MIN		
E4	1,8 MAX		
E5	4 ± 0,05		
E6	M1,6		
E7	Ø 2,3 MAX		
E8	15° ± 1°		
E9	Ø 3,28 MAX		
E10	4		
E11	5,08		
E12	4,63 ± 0,03		
E13	14,35		
E14	8,43 ± 0,05		

LABEL	DIMENSION	TOLERANCE	VALUE
E15	R1,65 ± 0,05		
E16	30° ± 0,05		
E17	3		
E18	3,81		
E19	19,9 MAX		
E20	1,1		
E21	7,8 MAX		
E22	4,73 MAX		
E23	0,45 MAX		
E24	1,4 MAX		
E25	4,1 ± 0,23		
E26	Ø 0,63 MIN		
E27	Ø 0,48 MAX		
E28	Ø 0,92 MIN		

Figure 38 - External micro-miniature D device connector interface



LABEL	DIMENSION	TOLERANCE	VALUE
G1	4		
G2	5.08		
G3	4.78 ± 0.05		
G4	14.35		
G5	8.55 ± 0.05		
G6	3.30 ± 0.02		
G7	R1.72 ± 0.05		
G8	R1.70 ± 0.05		
G9	29° ± 0.05°		

LABEL	DIMENSION	TOLERANCE	VALUE
G10	3		
G11	3.81		
G12	19.9 MAX		
G13	8.5 MAX		
G14	1.1		
G15	7.9 ± 0.1		
G16	1.7 MAX		
G17	3.8 MIN		
G18	Ø 0.57 ± 0.01		

Figure 39 - External micro-miniature D cable connector interface

8.5.1.5 Micro-miniature D external device connector pinout

The pinout for external device connectors is shown in Table 20.

Table 20 - External micro-miniature D device connector pinout

Pin	Signal	Notes
1	reserved	No connect
2	LineOut-	
3	Logic ground	Shall not connect directly to any cable shield or drain wire. Connection to a separate cable conductor is optional.
4	LineIn-	
5	Ground	Return for pin 8. If optional power is not provided on pin 8, then pin 5 shall be a no connect.
6	LineOut+	
7	reserved	No connect
8	+5 V ±5% (optional)	If supplied shall be capable of supplying a minimum of 0,25 A and a maximum of 1,0 A. Direct shorts to ground shall not cause damage. If optional power is not provided on pin 8, then pin 8 shall be a no connect.
9	LineIn+	
Shield	Shield	Shall conform to 8.5.4. Shield connection shall make before any other pin upon insertion.
NOTE - Pins 1, 3, 5, 7, and 8 shall not be connected between nodes.		

8.5.1.6 Micro-miniature D external cable pinouts

The pinout for external cable device connectors is shown in Table 21.

Table 21 - External micro-miniature D cable pinouts

Wire Color (optional)	Receptacle 1		Receptacle 2	
	Pin	Signal name	Pin	Signal name
Green	2	LineOut-	4	LineIn-
Red	6	LineOut+	9	LineIn+
White	4	LineIn-	2	LineOut-
Blue	9	LineIn+	6	LineOut+
Shield	Shield	Shield	Shield	Shield
NOTE - Pins 1, 3, 5, 7 and 8 are not normally connected (see Table 20).				

8.5.2 External HSSDC connector

The HSSDC external connector[1] is a polarized eight (8) position, fully shielded interconnect for high speed data transfer. It is impedance controlled by design for 150 Ω differential systems.

The contact interface is sequenced with make first, break last pins 2 and 7.

8.5.2.1 HSSDC shielding and retention schemes

The external HSSDC connectors are fully shielded for protection against RFI/EMI. Shield contact between the device and cable connectors is accomplished by nine (9) spring fingers on the device connector (three on each side, two on top and one on bottom).

a) External node connections shall provide a separate shielded device connector for each. The connector shield shall be grounded to the node enclosure in a manner that allows the connector system to satisfy the requirements in 8.5.4.

[1] For informational purposes, the HSSDC connector family is in the process of becoming an EIA standard via the SFF committee.

b) The external Cable Assembly shall be terminated with a shielded cable connector having a metallic shield and a backshell that connects the connector shield to the cable shield in a manner that allows the mated connector system to satisfy the requirements in 8.5.4.

The details of the shielded device connector mating interface are shown in Figure 41 the shielded cable in Figure 41.

The retention scheme is a positive latch. Retention forces shall be defined as forces on the cable media in a direction perpendicular to the plane of the enclosure wall that is securing the shielded device connector. The Cable Assembly shall withstand a maximum and minimum axial forces of 80 N and 45 N respectively.

8.5.2.2 HSSDC cable connector termination

Any termination technique may be used that allows the final product to meet the performance and dimensional requirements.

8.5.2.3 HSSDC contact finish on mating surfaces of connector contacts

The contacts are leaf style.

The electroplated finish on the mating surfaces shall ensure the compatibility of connectors from different sources. The following examples are compatible electroplatings and may be used on mating surfaces of contacts:

a) 0,76 μm (30 μin) minimum gold over 1,27 μm (50 μin) minimum nickel;
b) 0,05-0,127 μm (2-5 μin) gold over 0,76 μm (30 μin) minimum palladium over 1,27 μm (50 μin) minimum nickel;
c) 0,05-0,127 μm (2-5 μin) gold over 0,76 μm (30 μin) minimum palladium nickel alloy (80%Pd-20%Ni), over 1,27 μm (50 μin) minimum nickel;
d) or 0,1 μm (4 μin) minimum gold over 1,27 μm (30 μin) minimum palladium nickel alloy(80%Pd/20%Ni) over 0,5 μm (20 μin) minimum nickel.

8.5.2.4 HSSDC dimensional requirements

The external connectors shall be designed to meet the dimensional requirements defined in Figure 40 and Figure 41. These requirements are defined in order to ensure intermateability among different manufacturers.

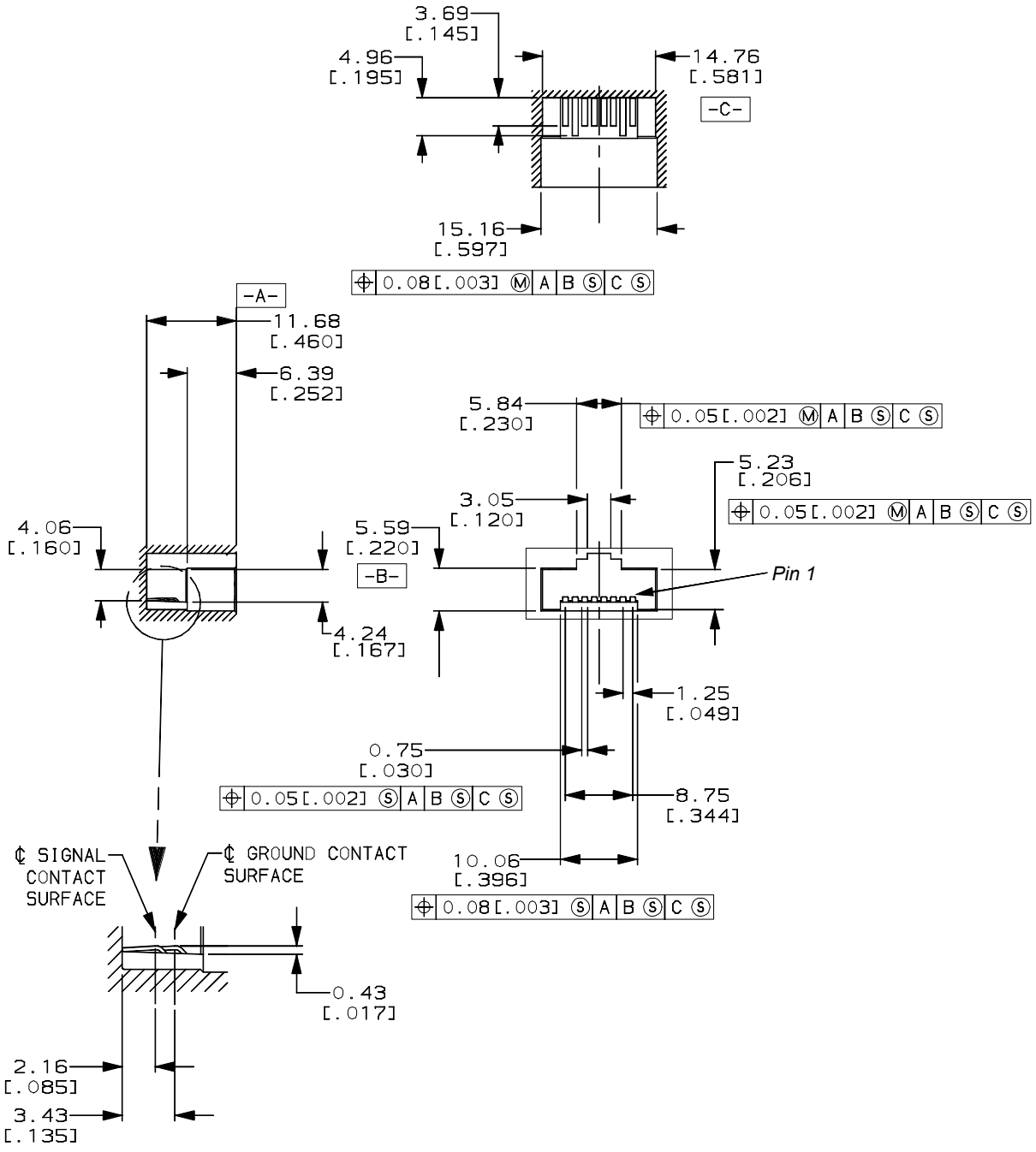


Figure 40 - External HSSDC device connector interface

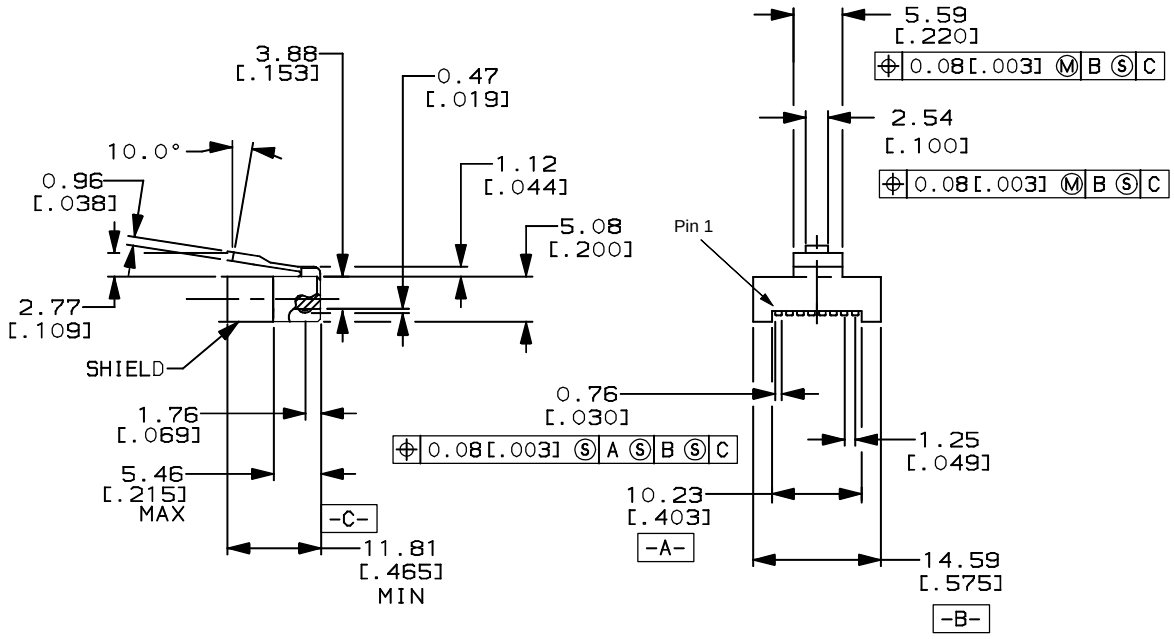


Figure 41 - External HSSDC cable connector interface

8.5.2.5 HSSDC external device connector pinout

The pinout for HSSDC external device connectors is shown in Table 22.

Table 22 - External HSSDC device connector pinout

Pin	Signal	Notes
1	LineOut+	
2	Ground	Return for pin 7. If optional power is not provided on pin 7, then pin 2 shall be a no connect. Pin 2 has a longer leaf for mate first break first capability.
3	LineOut-	
4	Logic ground	Shall not connect directly to any cable shield or drain wire. Connection to a separate cable conductor is optional.
5	reserved	No connect.
6	LineIn-	
7	+5 V ±5% (optional)	If supplied shall be capable of supplying a minimum of 0,25 A and a maximum of 1,0 A. Direct shorts to ground shall not cause damage. If optional power is not provided on pin 7, then pin 7 shall be a no connect. Pin 7 has a longer leaf for mate first break last capability.
8	LineIn+	
Shield	Shield	Shall conform to 8.5.4. Shield connection shall make before any other pin upon insertion.
NOTE: Pins 2, 4, 5, and 7 shall not be connected between nodes.		

8.5.2.6 HSSDC external cable pinouts

The pinout for HSSDC external cable device connectors is shown in Table 23.

Table 23 - External HSSDC cable pinouts

Wire Color (optional)	Receptacle 1		Receptacle 2	
	Pin	Signal name	Pin	Signal name
Green	3	LineOut-	6	LineIn-
Red	1	LineOut+	8	LineIn+
White	6	LineIn-	3	LineOut-
Blue	8	LineIn+	1	LineOut+
Shield	Shield	Shield	Shield	Shield
NOTE - Pins 2, 4, 5, and 7 are not normally connected (see Table 22).				

8.5.3 External cable media

An external cable shall contain at least 5 conductors: a pair of wires for the LineOut signals, a pair for the LineIn signals and a shield. See 7.5 for additional requirements.

NOTE 9 - Figure 42 shows one type of construction that may be used. In this construction, each pair of differential signals (LineOut/LineIn) is allocated to diagonally opposite wires. This minimizes cross-talk without the need to shield each pair individually. The geometrical arrangement of the 4 wires is controlled by the central filler and the overall shielding/jacket. The 4 wires are wrapped in an overall shield of aluminum/polyester tape. Consecutive turns overlap by 25% and the aluminum side of the tape faces out. This is followed by an overall braid shield with a minimum coverage of 85%. Finally, the cable is protected by a black PVC jacket with a thickness of 0,635 mm (0,025 inches). The braid shield is connected to frame ground at both ends via the connector shields.

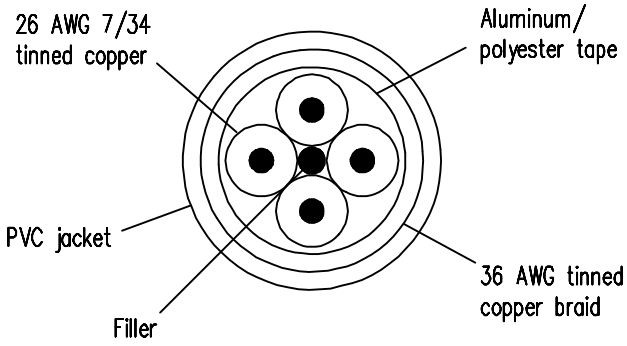


Figure 42 - Typical construction of external cable

8.5.4 Shield effectiveness

All external SSA connections shall meet the shield effectiveness requirements. The requirements are based on transfer impedance testing of the mated connection system. This system includes connectors, backshells, bulkhead mounting means, connector securing means, cable shield connections to the connector shield and any other parts used to accomplish the complete shield circuit connection from the cable shield to the enclosure wall.

The complete shielding system shall provide a d.c. resistance of less than 5 mΩ from the cable shield to the node enclosure.

Annex A contains a detailed description of a test procedure that shall be used to measure the transfer impedance of the connection system. The test results from this procedure shall not exceed the levels defined in Table 24.

Table 24 - Transfer impedance requirements for external SSA connections

Frequency (MHz)	Value (dB-Ω)(max)
30	-25
159	-16
500	-10

Annex A
(normative)
Transfer impedance testing procedure

A.1 Content

This requirement allows the transfer impedance (Zt) of electrical connectors to be determined from d.c. to 500 MHz. It measures the leakage of connector assemblies located between a bulkhead and a shielded cable.

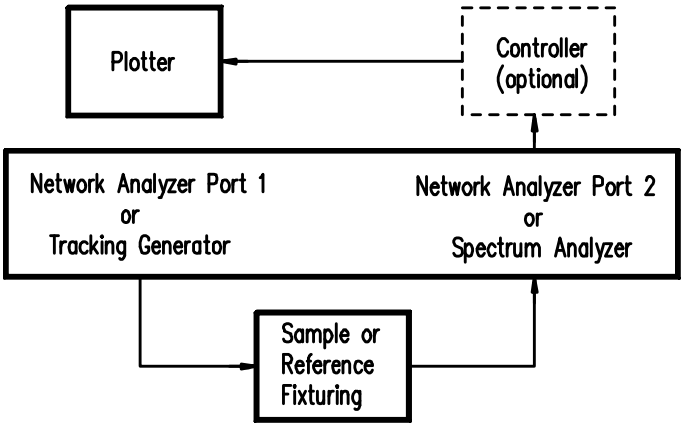


Figure A.1 - Test Equipment Block Diagram

A.2 Definitions

a) Connector Transfer Impedance (Zt): Connector transfer impedance is the ratio of the longitudinal voltage that appears on the outside of the connector under test to a known common mode current impressed on the inside conductors.

b) Units (dB-Ω) Measured results shall be reported in dB from one Ω [dB=20 log(Zt(1 Ω))]. More negative values represent better performance. Zero dB is one Ω. Positive results represent insignificant shielding. Each 20 dB represents a 10 fold change in transfer impedance.

A.3 Test equipment

A vector or scalar network analyzer shall be used. A spectrum analyzer and tracking generator may be used if provision has been made for dividing the magnitudes of two traces (subtracting in dB). Equipment shall be capable of generating plots directly or from magnetic media.

A.4 Theory

A.4.1 Reference measurement

This technique relies on comparing two measurements that differ only in where the drive energy is placed. In the reference measurement (see Figure A.2), the radio frequency (RF) current flows through the one Ω standard. The resulting voltage drives the sample on the outside, and the resulting power is measured at port 2 [or, this may be measured as S21 (reference)]. This voltage is equal to the voltage that is generated if the sample had a one Ω transfer impedance at all frequencies.

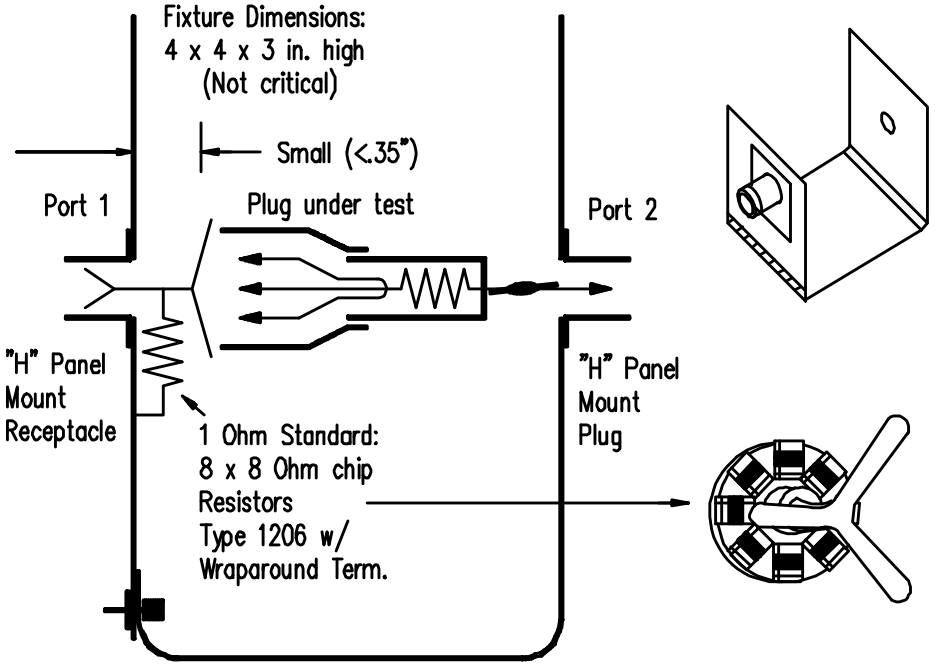


Figure A.2 - Reference measurement fixturing

This simple resistance is made to mimic a transfer impedance. Thus, the reference measurement only includes the fixturing response when the sample is mounted in it.

A.4.2 Sample measurement

The second measurement (see Figure A.3) applies the same amount of incident RF Power to the inside of the sample. The fixturing has exactly the same dimensions. The current from this incident power passes through the connector under test transfer impedance, producing a voltage along the length of the sample. The resulting power is measured at port 2 of Figure A.3 (or this may be measured as S21(sample)). This measurement includes the fixturing response previously measured times the transfer impedance of the sample.

A.4.3 Calculations

The transfer impedance may be derived from these two measurements. The sample measurement results are divided by the reference results at each frequency (subtract dB), leaving just the sample transfer impedance. The results shall be multiplied by a frequency independent correction factor (CF). Even with identical RF drive levels, the current through the one Ω standard of the reference measurement differs from the inside current of the sample measurement.

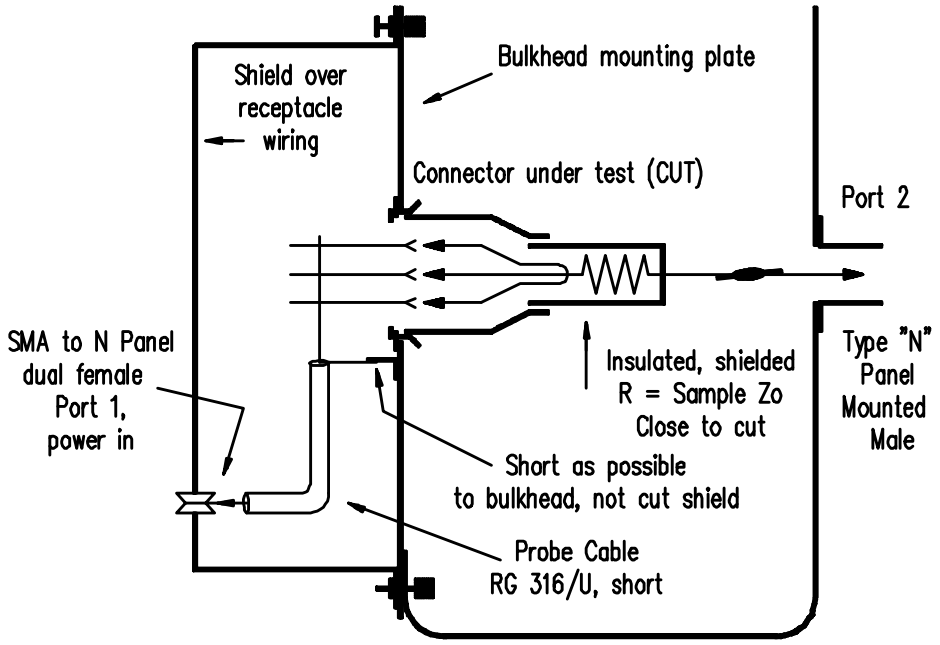


Figure A.3 - Sample measurement fixturing

A.5 Sample preparation

A.5.1 Panel mounted connector sample

The panel mounted connector sample shall be prepared in order as follows:

a) Mount connector in the center of a bulkhead mounting plate (Figure A.3);
b) Common all contacts as close to the bulkhead as possible;
c) A 1 inch wide copper strap shall be soldered to the bulkhead mounting plate close to the CUT;
d) The free end should be very close to the bussed panel mount connector conductors;
e) The shield of a short probe cable shall be soldered to the strap to form a low inductance path to the bulkhead, not the panel mount connector shield, and this connection should be as short as possible;
f) Solder the center conductor to the bussed panel mount connector conductors, this connection should be as short as possible;
g) Assemble the fixturing of Figure A.3;
h) Be sure metal surfaces joined are clean for a good connection.

A.5.2 Measure sample Zo with TDR

Measure sample Zo with a TDR in order as follows:

a) A sample connector shall be mounted on several inches of shielded cable;
b) All conductors in this connector shall terminate a conductor in the cable;
c) Mate to panel mounted connector sample (see A.5.1);
d) Use time domain reflectometry (TDR) to determine the voltage reflection coefficient of the mated pair;
e) Estimate an average value if necessary to be used to calculate a correction factor (CF).

A.5.3 Cable Mounted Connector Sample

The cable mounted connector sample shall be prepared as follows:

a) Cut the cable on each sample about 1 inch from the rear;

b) Remove the outer jacket without nicking the braid, leaving 0,2 inch of outer jacket;
c) Fold back braid over remaining outer jacket;
d) Remove second foil shield if present;
e) Take care to avoid stressing the connector shield braid capture region;
f) Strip all internal conductors to as close to the braid as practical;
g) Twist together all internal conductors and solder;
h) Cut soldered wires to 0,1 inch;
i) Solder a non-inductive (metal film) termination resistor to this;
j) Wrap this joint with high temperature insulating tape (Kapton);
k) The termination resistor shall be chosen to give a voltage reflection coefficient close to that measured in A.5.2 above;
l) Wrap the joint and termination resistor with copper tape;
m) Dress the braid up over the copper tape;
n) Wrap the braid and copper tape up to the free resistor lead with small gauge solid hook-up wire;
o) Solder these together to prevent any RF leakage.

A.6 Procedure

The Transfer Impedance Testing procedure shall be done in order as follows:

a) Do a full 2 port calibration if using a vector network analyzer for improved accuracy.
b) Get a noise floor plot (see A.7).
c) Prepare panel mounted connector sample(s) (see A.5.1)
d) Measure sample Zo (see A.5.2). Note the reflection coefficient p for use in step 8.
e) Prepare cable mounted samples (see A.5.3).
f) Do a reference measurement (see A.4.1). Solder the electrical connection at the right so that pressure is applied at the mechanical connection at the left (the fixture connection to the mating interface). Measure S21(reference) expressed in dB, or measure the power at the spectrum analyzer in dBm. The frequency range shall include 30 MHz to 500 MHz but may include more.
g) Do the sample measurements (see A.4.2). With the same cables, substitute the sample measurement fixturing of Figure A.3 for the reference measurement fixturing of step 6 (Figure A.3). Mate the connectors under test and connect to the type "N" connector at the right. Measure S21 (sample) expressed in dB, or measure the power at the spectrum analyzer in dBm while driving the sample with the same forward power (into fixture port 1, Figure A.3) as used in step 6.
h) Calculate the correction factor. In dB it is: CF(dB) = 20 log(2/(1-p)), where p is the voltage reflection coefficient of the termination resistor, determined in step 4 above (see A.5.3).
i) The vertical axis of the trace may now be labeled in units of dB-Ω: Zt(dB-Ω) = dBm(sample) - dBm(reference) + CF(dB) = S21(sample) - S21(reference) + CF(dB), where S21 is expressed in dB. Note that the subtraction above may be done by many instruments in real time. If so, the reference graticule of the subtracted results may be assigned a value of (-1)CF(dB), that makes it equal to 0 dB-Ω. Or, a controller may do these calculations.
j) Plot transfer impedance in log log format, save plot file and record single frequency results.
k) Check that all points on the transfer impedance plot (trace) exceed the noise floor plot (see A.7) by at least 10 dB. Note invalid regions in the plot data.

A.7 Noise floor plot

If the samples have very good shielding, the fixturing shielding may be inadequate, or the receiver may be picking up ambient signals. Before samples are measured, some idea of this level shall be available. This shall be obtained with the noise floor plot fixturing of Figure A.4.

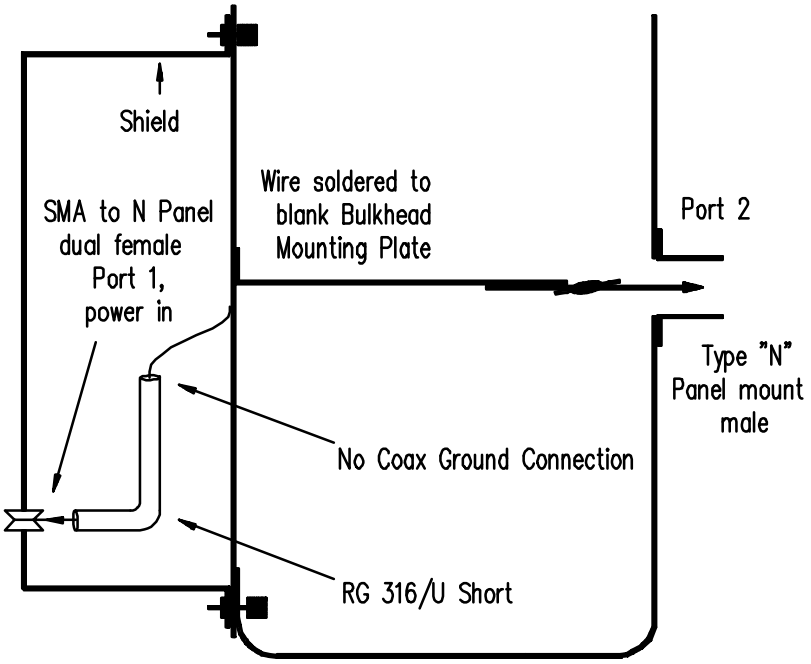


Figure A.4 - Noise floor check fixturing

The noise floor plot is obtained just like a transfer impedance measurement but with a solid panel and no connector under test. A reference measurement is first made using a wire instead of a cable mounted sample. The sample measurement is made as in Figure A.4. The sample measurement is then divided by the reference measurement (subtract dB). All transfer impedance data that does not exceed this ratio by at least 10 dB shall be reported as inaccurate data.

A.8 Documentation

A.8.1 Plots and magnetic files

a) Company name.
b) Test Number
c) Date.
d) Sample identification and test conditions.
e) Correction factor in dB, or termination resistance used.

A.8.2 Test report

a) Plots, if requested (log log format, including 30-500 MHz data).
b) Single frequency results (30 and 159 MHz recommended).
c) Noise floor plot. Document any data that fails the noise floor requirement.
d) Equipment used.
e) Termination resistor values used.

Annex B
(normative)
Internal connector testing procedure

To verify the performance requirements, performance testing is defined according to the recommendations, test sequences and test procedures of ANSI/EIA 364. ANSI/EIA 364 defines operating class definitions for different end-use applications.

SSA internal connector test requirements follow the recommendations for environmental class 1.3, defined as: No air conditioning or humidity control with normal heating and ventilation. The Equipment Operating Environmental Conditions shown, for class 1.3 in table 2 of ANSI EIA 364 are: Temperature; +15 degrees C to +85 degrees C, Humidity; 95% maximum., Class 1.3 is further described as operating in a harsh environmental state, but with no marine atmosphere.

Accordingly, the performance groupings, sequences within each group, and the test procedures follow the recommendations of ANSI/EIA 364, except where the unique requirements of the SSA internal connectors may call for tests that are not covered in ANSI/EIA 364, or where the requirements deviate substantially from those in that document. In those cases, test procedures of other recognized authorities are cited.

All internal connectors described in Figure B.1 shall pass all the following tests, in the groups, and sequences shown, and in the sample sizes shown.

B.1 Test sample preparation

The internal connectors shall be tested unassembled for those tests that require it. They shall be tested assembled to randomly selected production printed wiring boards or cable assemblies, typical of those used in SSA equipment, for those tests that require assembled connectors

a) All performance testing is to be done with cable material that conforms to this requirement. In order to test to these performance groups, EIA tests require that the cable construction used be pacified.

b) All resistance values shown in the following performance groups are for connectors only, including their termination to the wire and/or PC board, but excluding the resistance of the wire. Resistance measurements shall be performed in an environment of temperature, pressure and humidity defined by EIA 364.

c) The numbers of units to be tested is a minimum; the actual sample size is to be determined by requirements of users. This is not a qualification program.

d) See Figure B.1 for contact resistance measurement points.

e) If non-unitized device connectors are used they shall be treated in the same manner as defined for the unitized device connectors in the tests except that tests with the unitized backplane connector are not required. Non-unitized device connectors are not specifically called out in these tests

B.2 Performance group A: Basic functionality - to mechanical shock and vibration

Performance group A refers to basic mechanical conformance and electrical functionality when subjected to mechanical shock and vibration.

The number of samples used is:

a) [2] 38 contact unitized device connectors, unassembled to PCB used for Phase A1 and A2 (one each);
b) [4] 38 contact unitized device connectors, assembled to PCB;
c) [2] 38 contact unitized backplane connectors, assembled to PCB;
d) [2 each] 16, 10 and 6 contact cable connectors, assembled to a 200 mm long cable.

Table B.1 - Performance group A

	Test conditions			Measurements to be performed		Requirements
Phase	**Title**	**ID No.**	**Severity or conditions**	**Title**	**ID No.**	**Performance Level**
A1	Visual and dimensional	ANSI/EIA 364-18	Unmated connectors	Dimensional Inspection	Figure 20 through Figure 37	No defects that impairs normal operations. No deviation from dimensional tolerances.
A2	Plating thickness measurement					Record thickness; see 8.1.4
A3	None		See Figure B.1	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum, initial per contact pair. (each contact)
A4	Vibration	ANSI/EIA 364-28	Cond. III [1]	Continuity	ANSI/EIA 364-46	No discontinuity of 1 μs or longer (each contact)
A5	None		Same as A3	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum change from original per contact pair. (each contact)
A6	Mechanical shock (defined pulse)	ANSI/EIA 364-27	Condition G [1]	Continuity	ANSI/EIA 364-23	No discontinuity at 1 μs or longer (each contact)
A7	None		Same as A3	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum change from original per contact pair. (each contact)

NOTE [1] - Connectors are to be mounted on a fixture that simulates typical usage. The PCB shall also be permanently affixed to the fixture. The PCB layout used represents actual use. The cable connector shall be mated with the plug, and the other end of the cable shall be permanently clamped to the fixture.

B.3 Performance group B: Contact resistance with thermal shock and humidity stress

Performance group B refers to low level contact resistance when subjected to thermal shock and humidity stress.

The number of samples used is:

a) [4] 38 contact unitized device connectors, assembled to PCB;
b) [2] 38 contact unitized backplane connectors, assembled to PCB;
c) [2 each] 16, 10, 6 contact cable connectors, assembled to cable, 200 mm long.

Table B.2 - Performance group B

	Test conditions			Measurements to be performed		Requirements
Phase	**Title**	**ID No.**	**Severity or conditions**	**Title**	**ID No.**	**Performance level**
B1	None		See Figure B.1	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum, initial, per contact mated pair (each contact)
B2	Thermal Shock	ANSI/EIA 364-32	Condition 1: 10 cycles (mated)	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum change from original per contact mated pair (each contact)
B3	Humidity	ANSI/EIA 364-31	Condition C: (504 hrs.) Method III (cycling) non-energized Commit 7A & 7b (mated)	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum change from original per contact mated pair (each contact)

B.4 Performance group C: Insulator integrity with thermal shock and humidity stress

The number of samples used is:

a) [4] 38 contact unitized device connectors, assembled to PCB;

b) [2] 38 contact unitized backplane connectors, assembled to PCB;

c) [2 each] 16, 10 and 6 contact cable connectors, unassembled.

Table B.3 - Performance group C

	Test conditions			Measurements to be performed		Requirements
Phase	**Title**	**ID No.**	**Severity or conditions**	**Title**	**ID No.**	**Performance Level**
C1	With-standing voltage	ANSI/EIA 364-20	Test voltage 500 V d.c. ± 50V Method C Unmated and unmounted	With-standing voltage	ANSI/EIA 364-20	No flashover No sparkover No excess leakage No breakdown
C2	Thermal Shock	ANSI/EIA 364-32	Condition 1 10 cycles (unmated)	With-standing voltage (same condition as C1)	ANSI/EIA 364-20	No flashover No sparkover No excess leakage No breakdown
C3	Insulation resistance	ANSI/EIA 364-21	Test voltage 500 VDC ± 50V Unmated and unmounted	Insulation resistance	ANSI/EIA 364-21	1 GΩ, minimum, between adjacent contacts
C4	Humidity (cyclical)	ANSI/EIA 364-31	Condition A (96 hours) Method III non-energized Omit 7a & 7b	Insulation resistance (same conditions as C3)	ANSI/EIA 364-31	1 GΩ, minimum, between adjacent contacts

B.5 Performance group D: Contact life with corrosive gas exposure

Performance group D refers to contact life and durability when subjected to mechanical cycling and corrosive gas exposure.

The number of samples used is:

a) [4] 38 contact unitized device connectors, assembled to PCB;

b) [2] 38 contact unitized backplane connectors, assembled to PCB;

c) [2 each] 16, 10 and 6 contact cable connectors, assembled to cable, 200 mm long.

Table B.4 - Performance group D

	Test conditions			Measurements to be performed		Requirements
Phase	**Title**	**ID No.**	**Severity or conditions**	**Title**	**ID No.**	**Performance Level**
D1	None		See Figure B.1	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum change from original per contact mated pair (each contact)
D2	Durability	ANSI/EIA 364-09	a) 2 mated pairs, 5 cycles b) 2 mated pairs, automatic cycles to 250 cycles, rate 500 cycles/hr ± 50 cycles			
D3	None		See Figure B.1	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum change from original per contact mated pair (each contact)
D4	Mixed flowing gas	ANSI/EIA 364-65 Class II	See Figure B.1 2 mated pairs-unmated for 1 day. 2 mated pairs mated for 10 days	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum change from original per contact mated pair (each contact)

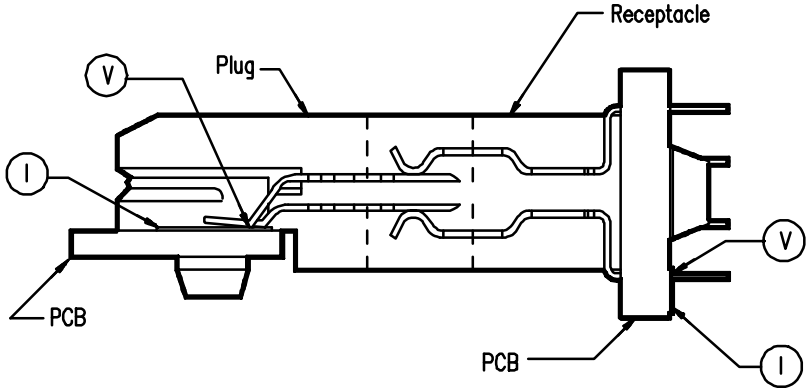


Figure B.1 - Contact resistance measuring points

B.6 Performance group E: Contact resistance with temperature life stress

Performance group E refers to contact resistance and mating and unmating force when subjected to temperature life stress.

The number of samples used is:

a) [4] 38 contact unitized device connectors, assembled to PCB;
b) [2] 38 contact unitized backplane connectors, assembled to PCB;
c) [2 each] 16, 10 and 6 contact cable connectors, assembled to cable, 200 mm long.

Table B.5 - Performance group E

	Test conditions			Measurements to be performed		Requirements
Phase	**Title**	**ID No.**	**Severity or conditions**	**Title**	**ID No.**	**Performance level**
E1	Mating and unmating	ANSI/EIA 364-13	Mating: Mount plug rigidly. Insert receptacle by hand			
			Unmating: Auto rate: 25 mm/min	Unmating only	ANSI/EIA 364-13	Unmating force: 1 kgf minimum 4 kgf maximum
E2	None	-	See Figure B.1	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum, initial per contact mated pair. (each contact)
E3	Temperature life	ANSI/EIA 364-17	Condition IV (105 degrees C) 250 hrs. Method A (mated). See Figure B.1	Low level contact resistance	ANSI/EIA 364-23	15 mΩ, maximum, change from original per contact mated pair. (each contact)
E4	Mating and unmating forces	ANSI/EIA 364-13	Same as E1	Mating and unmating forces	ANSI/EIA 364-13	Same as E1

B.7 Performance group F: Mechanical retention and durability

The number of samples used is:

a) [4] 38 contact unitized device connectors, assembled to PCB;
b) [2] 38 contact unitized backplane connectors, assembled to PCB;
c) [2 of each] 16, 10 and 6 contact cable connectors, assembled to cable 254 mm long minimum.

Table B.6 - Performance group F

	Test conditions			Measurements to be performed		Requirements
Phase	**Title**	**ID No.**	**Severity or conditions**	**Title**	**ID No.**	**Performance level**
F1	Mating and unmating forces	ANSI/EIA 364-13	Mating: Mount plug rigidly. Insert receptacle by hand			
F2	Mating and unmating forces	ANSI/EIA 364-13	Auto cycle: 100 cycles, 25 mm/min	Unmating forces	ANSI/EIA 364-13	Unmating force: 1 kgf minimum 4 kgf maximum
F3	Durability	ANSI/EIA 364-09	Auto cycling to 500 cycles	Unmating only	ANSI/EIA 364-13	Unmating force at end of durability cycling: 1 kgf minimum 4 kgf maximum

B.8 Performance group G: General test

Suggested procedures to test miscellaneous, but important aspects of the connectors.

NOTE 10 - Since the test listed below may be destructive, separate samples should be used for each test. The number of samples to be used is listed under the test title.

Table B.7 - Performance group G

	Test conditions			Measurements to be performed		Requirements
Phase	**Title**	**ID No.**	**Severity or conditions**	**Title**	**ID No.**	**Performance level**
G1	Cable axial pull test (2 device connectors)		Fix device connector housing and apply a 10 kgf load for one minute on cable axis	Continuity Visual	ANSI/EIA 364-46	No discontinuity greater than 1 μs. No jacket tears or visual exposure of shield. No jacket movement greater than 1,5 mm at point of exit.
G2	Cable flexing (2 device connectors)	ANSI/EIA 364-41	Condition I dimension x =3,7 x cable diameter or thickness; 100 cycles, in each of two planes	a) With-standing voltage	Per C1	Per C1
				b) Insulation resistance	Per C3	Per C3
				c) continuity of all contacts	Per A4	Per A4

Annex C
(normative)
External Micro-miniature D connector testing procedure

The clause defines the general test schedule. This test schedule shows all the tests and the order they shall be carried out as well as the requirements to be met. Unless otherwise defined, all tests shall be carried out under standard atmospheric conditions for testing as defined in IEC 68-1, as directed by the applicable IEC 512 documents. Unless otherwise defined, mated sets of connector pairs shall be tested. Care shall be taken to keep a particular combination of connector pairs together during the complete test sequence (i.e. when unmating is necessary for a certain test, the same connector pairs as before shall be mated the subsequent tests).

In the following, a mated set of connector pairs is called a specimen. When the initial tests have been completed, all the specimens are divided up according to the test groups.

Before testing commences, the connector pairs shall be stored for at least 24 hours in the non-inserted state under normal atmospheric conditions as per IEC 68-1.

The necessary specimens to perform the entire test program are stated in Table C.1.

Table C.1 - Number of test specimens

Testgroup		Number of specimens
Initial tests 8.5.4.2.1.	P 1	17
Testgroup 8.5.4.2.2.	AP	4
Testgroup 8.5.4.2.3	BP	4
Testgroup 8.5.4.2.4	CP	4
Testgroup 8.5.4.2.5	DP	4
NOTES 1) Initial tests P contain one reference sample 2) All testgroups are at performance level 1.		

C.1 Test group P - Initial Test

Table C.2 - Initial tests

Test Phase	Test conditions			Severity or condition of test	Measurement to be performed			Requirements
	Title	Test	IEC 512 part		Title	Test	IEC 512 part	
P1.1				Unmated connectors	Visual examination	1a	2	There shall be no defects that impairs normal operations.
P1.2				Unmated connectors	Examination of dimensions	1b	2	No deviations from dimensional tolerances
P2	Polarizing method	13e	7	Test force = 25 N maximum				It shall not be possible to mate connectors in any manner other than the correct one
P3				6 contacts per connector. See Figure C.2 for measurement points	Contact resistance	2a	2	35 mΩ maximum contact resistance for style B. 20 mΩ maximum for style C
P4				Test voltage 100 ± 15 V 3 contacts per connector	Insulation resistance	3a	2	Insulation resistance to be $> 5 \times 10^9\ \Omega$
P5				Apply 350 V a.c. minimum between adjacent contact rows and 500 V a.c. minimum between contacts and shell	Voltage proof	4a	2	There shall be no breakdown or flashover

C.2 Test group AP - Mechanical and thermal shock, vibration and humidity stress

Test group AP tests the contact resistance and insulator integrity using mechanical and thermal shock, vibration and humidity stress.

Table C.3 - Contact resistance and insulator integrity

Test Phase	Test conditions			Severity or condition of test	Measurement to be performed			Requirements
	Title	Test	IEC 512 part		Title	Test	IEC 512 part	
AP1				6 pin contacts per connector using gauge per Figure C.4	Gauge retention force	16e	8	0,15 N minimum withdrawal force
AP2				Insertion and withdrawal force	Connector mating and unmating force	13a	7	25 N maximum mating force.
AP3	Solderability	12a	6	Applies to solder pin termination only. Completely dip solder tails in solder bath	Visual Examination			There shall be no evidence of dewetting. Contact surface shall be fully and evenly coated with solder.
AP4				Apply 350 V a.c. minimum between adjacent contact rows and 500 V a.c. minimum between contacts and shell	Voltage proof	4A	2	There shall be no evidence of breakdown or flashover
AP5	Vibration	6d	4	Freq. = 10-32 Hz, amplitude=,35mm Freq=32-500 Hz, Accel. = 5gs, Duration = 6 hrs. Connector mounting per Figure C.2.	Contact resistance Contact intermittence	2a 2c	2 2	Maximum 15 mΩ change from initial contact resistance measured in Table C.2 test P3. Contact intermittencies to be less than 1 μs. Intermittency defined to be a contact resistance greater than 500 Ω
AP6	Mechanical shock	6c	4	Acceleration 50g duration 11 ms 10 shocks, 5 in each direction half sine Connector mounting per enclosed figure.	Contact resistance Contact intermittence	2a 2c	2 2	Maximum 15 mΩ change from initial contact resistance measured in Table C.2 test P3. Contact intermittencies to be < 1 μs Intermittency defined to be a contact resistance > 500 Ω.
AP7	Thermal shock	11d	6	test Na; duration: 30 min. Temperature - -55 to +125 Celsius				
AP8				Test voltage 100 ± 15 V 3 contacts per connector	Insulation resistance	3a	2	Insulation resistance greater than $5x10^{9}\Omega$

Test Phase	Test conditions			Severity or condition of test	Measurement to be performed			Requirements
	Title	Test	IEC 512 part		Title	Test	IEC 512 part	
AP9				Apply 350 V minimum between adjacent contacts rows and 500 V minimum between contacts and shell.	Withstanding voltage	4a	2	There shall be no evidence of breakdown or flashover
AP10				Unmated connectors	Visual examination	1a	2	There shall be no damage that impairs normal operation.
AP 11	Climatic sequence	11a	6	See AP11.1-AP11.4				
AP11.1	Dry heat	11i	6	Unmated connectors duration: 12h @ 125°C recovery time: 2h	insulation resistance (hot)	3a	2	Insulation resistance to be $>1x10^8\ \Omega$ at 125°C.
AP11.2	damp heat cyclic, first cycle	11m	6	above temperature 40°C, recovery time: 2h variance 2				
AP11.3	cold	11j	6	-55°C, duration: 6h recovery time: 2h				
AP11.4	damp heat, cyclic remaining (5) cycles	11m	6	above temperature 40°C, recovery time: 2h variance 2				
AP 12				for arrangement and test condition see P4	Insulation resistance	3a	2	Insulation resistance to be $>5 \times 10^9\Omega$
AP 13				6 contacts per connector. Measurement points to be per Figure C.2	Contact resistance	2a	2	Maximum 15 mΩ change from initial contact resistance measured in Table C.2 test P3.
AP 14				test conditions see P5	Withstanding voltage	4a	2	There shall be no evidence of breakdown or flashover.
AP15				Insertion and withdrawal force = 25 N maximum	Total mating + unmating forces	13a	7	
AP16				Unmated connectors	Visual examination	1a	2	There shall be no damage that impairs normal operation

C.3 Test group BP - Mechanical cycling and corrosive gas exposure

Test group BP refers contact life and durability testing using mechanical cycling and corrosive gas exposure.

Table C.4- Contact life and durability - mechanical cycling and corrosive gas exposure

Test Phase	Test conditions			Severity or condition of test	Measurement performed			Requirements
	Title	Test	IEC 512 part		Title	Test	IEC 512 part	
BP1				6 pin contacts per connector using gauge per Figure C.4	Pin contact withdrawal force	16e	8	0,15 N minimum withdrawal force
BP2	Durability	9a	5	Speed 10 mm/s. Rate = 2 cycles/minute 500 cycles, - 30 second rest period in the unmated condition				
BP3	Industrial gas	11g	11-7	Half connectors mated Half connectors unmated test condition A(SO2)				4 days duration
BP4				6 contacts per connector Measurement points to be per Figure C.1	Contact resistance	2a	2	Maximum 15 mΩ change from initial contact resistance measured in Table C.2 test P3.
BP5	Durability	9a	5	Speed 10 mm/s. Rate = 2 cycles/minute, 500 cycles. The last 10 mating operations by hand. 30 second rest period in unmated condition				
BP6				Test voltage = 100 ± 15 V 3 contacts per connector	Insulation resistance	3a	2	Insulation resistance to be > $5x10^{9}\Omega$
BP7				Apply 350 V a.c. min. between adjacent contact rows and 500 V a.c. min. between contacts and shell.	Voltage proof	4a	2	There shall be no evidence of breakdown or flashover
BP8				6 pin contacts per connector using gauge per Figure C.4	Pin contact withdrawal force	16e	8	0,15 N minimum withdrawal force
BP9				Unmated connectors	Visual examination	1a	2	There shall be no damage that impairs normal operation
BP10	Static load, axial	8b	5	Number of samples : 2 connectors. Load to be applied as shown per Figure C.3. Application rate = 10 N/s. Total force = 25 N minimum				There shall be no damage that impairs normal operation

C.4 Test group CP - Contact resistance and insulator integrity - humidity stress

Table C.5 - Contact resistance and insulator integrity - humidity stress

Test Phase	Test conditions			Severity or condition of test	Measurement to be performed			Requirements
	Title	Test	IEC 512 part		Title	Test	IEC 512 part	
CP1	Humidity	11c	6	Applied voltage to be 60 V d.c. 2h drying time 21 day duration See Figure C.1 for test points.				
CP2				Test voltage = 100 ± 15 V. 3 contacts per connector	Insulation resistance	3a	2	Insulation resistance to be greater than 10^7 Ω
CP3				6 contacts per connector. Measurement points to be per Figure C.1	Contact resistance	2a	2	Maximum 15 mΩ change from initial contact resistance measured in Table C.2 test P3.
CP4				Apply 350 V a.c. minimum between adjacent contacts rows and 500 V a.c. minimum between contacts and shell	Withstanding voltage	4a	2	There shall be no evidence of breakdown or flashover
CP5				Unmated connectors	Visual examination	1a	2	There shall be no damage that impairs normal operation

C.5 Test group DP - Contact life and durability - mechanical cycling

Table C.6 - Contact life and durability - mechanical cycling

Test Phase	Test conditions			Severity or condition of test	Measurements performed			Requirements
	Title	Test	IEC 512 part		Title	Test	IEC 512 part	
DP1	Durability	9a	5	Speed 10 mm/s. Rate=2 cycles/minute, 500 cycles, rest 30 seconds unmated.				
DP2	Electrical load and temperature.	9b	5	55°C test temperature, 500 hours duration, 1.3A current, AWG 28 wire				
DP3				6 contacts per connector. Measurement points to be per figure 33.	Contact resistance	2a	2	Maximum 15 mΩ change from initial contact resistance measured in Table C.2 test P3.
DP4				Apply 350 V a.c. min. between adjacent contacts rows and 500 V a.c. min. between contacts and shell.	Voltage proof	4a	2	There shall be no evidence of breakdown or flashover
DP5				Test voltage 100 ± 15 V 3 contacts per connector	Insulation resistance	3a	2	Insulation resistance to be greater than $10^7\Omega$
DP8				Unmated connectors	Visual examination	1a	2	There shall be no damage that impairs normal operation

C.6 Performance test supplementary requirements

Figure C.1 applies to test phases P3, AP6, AP7, AP15, CP3 and DP3 for measurement of contact resistance. Current for testing 20 mA. Maximum voltage during testing shall not exceed 20 mV

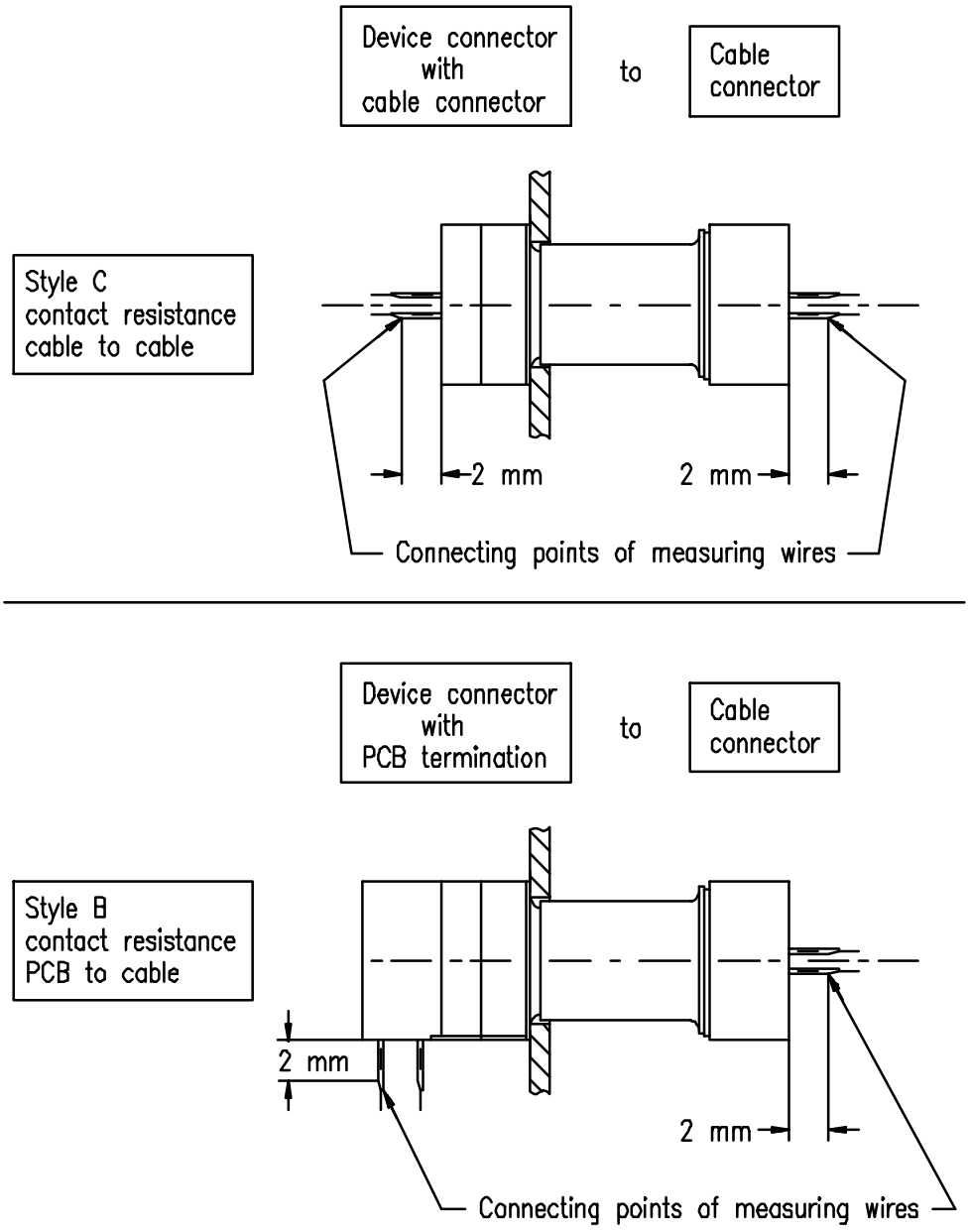


Figure C.1 - Test points for contact resistance measurements

Figure C.2 applies to test phases AP6 and AP7. All connector wires are fixed approximately 50 mm away from the cable exit.

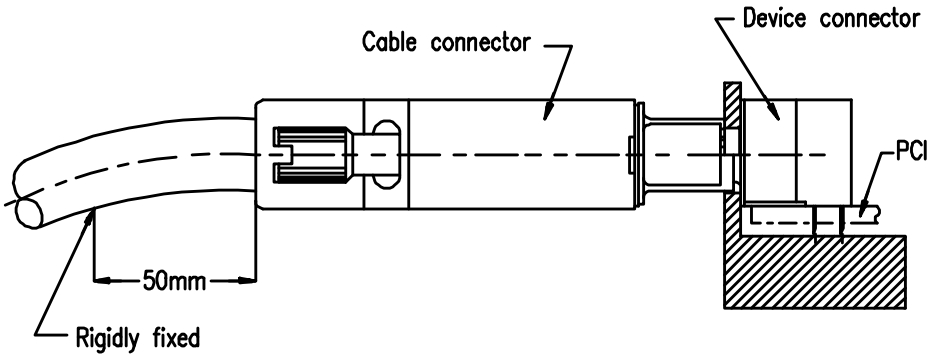


Figure C.2 - Test fixture for shock and vibration testing

Figure C.3 applies to test phase BP11.

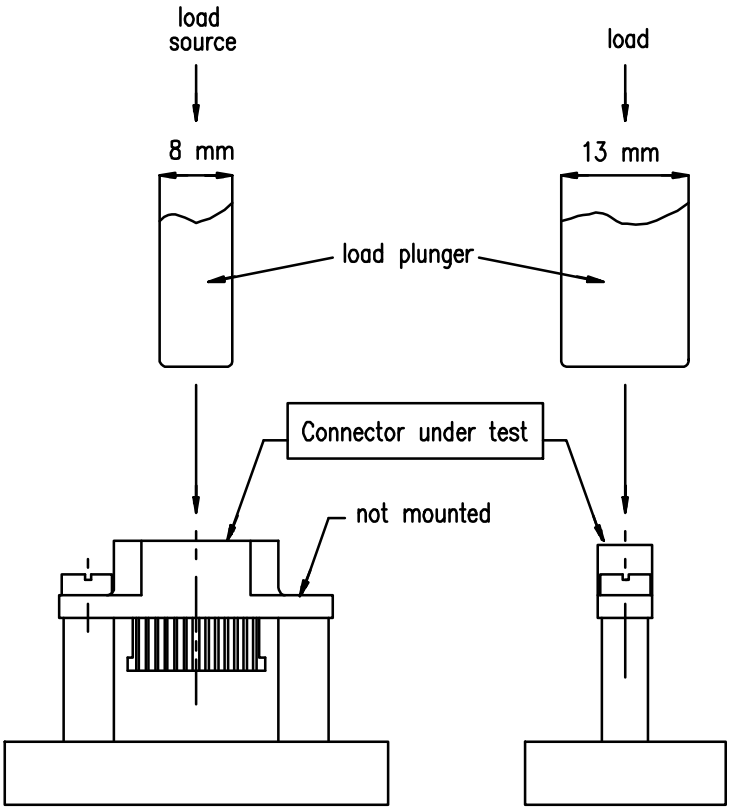
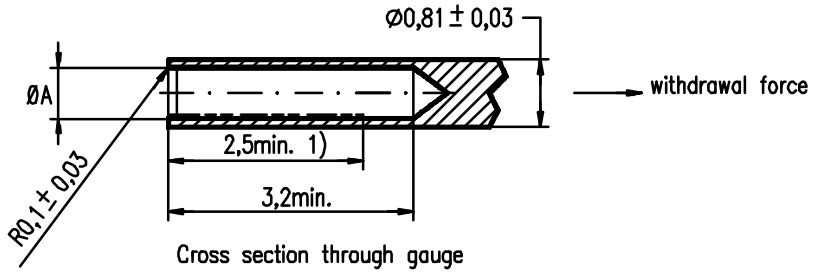


Figure C.3 - Arrangement for static axial load test

Figure C.4 applies to test phases AP1, BP1 and BP9. The materials shall have the following properties: Tool steel, 60 Rockwell C Min, 0.25 µm max finish over ∅A.

Gauge	ØA	Tolerance
Sizing gauge P1	0,561 mm	± 0,0025 mm
Test Gauge P2	0,584 mm	± 0,0025 mm



Test method for withdrawal force of individual contact
- 2x premating with P1
- withdrawal force with P2
- ≥ 0,15N

Figure C.4 - Gauge requirements for contact withdrawal force testing

Annex D
(normative)
External HSSDC connector testing procedure

Table D.1 - External HSSDC connector test procedure

TEST DESCRIPTION	REQUIREMENTS	PROCEDURE
Examination of product	Meets requirements of Figure 40 and Figure 41	Visual, dimensional, and functional per applicable quality inspection plan
Termination resistance	35 mΩ maximum (initial) resistance Δ = 25 mΩ maximum (final)	Subject mated connectors to 20 mV open circuit at 100 mA maximum per IEC 512-2 test 2a.
Insulation resistance	500 MΩ maximum (initial) 100 MΩ maximum (final)	Apply potential of 100 ± 15 V between adjacent contacts per IEC 512-2 test 3a.
Dielectric withstanding voltage	No breakdown or flash over permitted	Apply potential of 350 V a.c. between adjacent contact rows, 500 V a.c. minimum between contact and shell per IEC 512-2 test 4a.
Mating/unmating force	5 lb. maximum.	Measure force required to mate connector using a free floating fixture at rate of 25 mm per minutes per IEC 512-2 test 4a.
Solderability	Solderable area should have a minimum of 95% coverage	Subject contacts to Solderability test per IEC 512-6 test 12a.
Random vibration	No discontinuities greater than 1 microsecond, maximum 15 mΩ max ΔR from initial resistance.	Subject mated connectors to 10-32 Hz , amplitude = 0,35 mm, and 32 - 500 Hz, acceleration = 5gs for duration of 6 hours per IEC 512-4 test 6d.
Mechanical shock	No discontinuities greater than 1 microsecond, maximum 15 mW max DR from initial resistance.	Subject mated connectors to 50 g half sine shock pulses of 11 ms duration, 5 in each direction for a total of 10 shocks per IEC 512-4 test 6c.
Thermal shock	No physical damage.	Subject mated connectors to 5 cycles between -55°C and +125°C per IEC 512-6 test 11d.
Humidity & temperature cycling	Insulation resistance 100 MΩ maximum (final)	Subject mated connectors to 10 humidity-temperature, between 25°C and 65°C at 95% RH with cold shocks at -10°C per IEC 512-6 test 11c.
Durability	No physical damage 35 mΩ maximum (initial) resistance D = 25 mΩ maximum (final)	Mate and unmate connectors for 500 cycles at a rate of 2 cycles/minute with 30 second rest period between cycles for 500 cycles total per IEC 512-5 test 9a.
Industrial mixed flowing gas	No physical damage 35 mΩ maximum (initial) resistance Δ = 25 mΩ maximum (final)	Subject mated connectors to environmental class II for 20 days per IEC 512-11-7 test 11g method 2.
Humidity	No physical damage 35 mΩ maximum (initial) Δ = 25 mΩ maximum (final)	Subject mated connectors to steady state humidity at 40°C and 90-95% RH per IEC 512-6 test 11c.
Static load	No physical damage	Subject receptacle connector to a compressive axial load of 25 N, application rate of 10 n/second
Temperature life	No physical damage 35 mΩ maximum (initial) Δ = 25 mΩ maximum (final)	Subject mated connectors to temperature life at 55°C for 500 hours per IEC 512-5 test 9d.

Table D.2 - External HSSDC connector test sequence

Test Description	Test Group [1]			
	1	**2**	**3**	**4**
Examination of product	1,14,18	1,11	1,9	1,7,10
Termination resistance	2,16	2,7	2,7	2
Insulation resistance	3,12,15	3,9	3,6	3,9
Dielectric withstanding voltage	4,8,13,17	4,10	4,8	4,8
Random vibration	9			
Mechanical shock	10			
Mating force	5			
Unmating force	6			
Durability		5,8		5
Solderability	7			
Thermal shock	11			
Humidity & temperature cycling	14 [2]			
Mixed flowing gas		6		
Temperature life				6
Steady state humidity			5	
Static load		12		

NOTES
[1] - Numbers indicate sequence in which tests are performed.
[2] - Condition unmated connectors for 12 hours at 125°C (dry heat) before humidity-temperature test.

Annex E
(normative)
Nulling of intersymbol jitter

The scope trigger source used for the Pulse Mask testing does not allow the timings of Table 3 (for the driver) or Table 7 (for the receiver) to be used for varying data patterns, or directly used on data streams of one character value. This annex describes a method which enables these timings to be applied to the K28.5 character when the predominant jitter is intersymbol jitter.

Continuous contiguous K28.5 characters contain a pattern that repeats every 20 bits. A stable display of all 20 bits is obtained by adjusting the scope trigger parameters. The trigger is then being taken from the same bit. Thickening of traces at the zero crossing point in the time dimension is caused by random jitter. Data dependent jitter and amplitude remain in the waveform for comparison against the pulse mask requirement on a bit by bit basis.

The procedure for nulling intersymbol jitter may be performed as follows:

a) Trigger the scope as detailed in 0 but use a delay of 4 to 12 data bit times.
b) Adjust the scope timebase such that a total of 20 data bit times is displayed. A stable display of the K28.5 character should now be possible. Adjustment of trigger holdoff may be required.
c) Define a window or delayed sweep trace containing the Driver or Receiver Pulse Mask of Figure 9 or Figure 12 using the timings from Table 3 or Table 7 as required.
d) Check each data bit time of the main display by moving the window or delayed sweep in 1 data bit time intervals. Adjust the reference point, to which the 1 data bit time intervals are referenced, in increments of less than 1 data bit time, until a point is found at which all data bit times pass the mask without interim adjustment of the reference point, or no such point is found.

Annex F
(informative)
Line fault detection scheme example

The line receiver may indicate a line fault when the magnitude of the differential voltage at the input is less than a receiver line fault threshold (RLFT). A line fault should be detected within 22 ns. However the detector should not be so fast that the finite rise and fall times of a normal signal cause false indications.

The RLFT may be exceeded under the following conditions:

a) Both wires of the inbound line are open-circuit;

b) Both wires of the inbound line are shorted together;

c) The remote node is powered off.

Severe external noise and may cause transient Line-fault indications. The RLFT is greater than ± 50 mV and less than ± 100 mV differential.

Annex G
(informative)
Circuit for degrading signal amplitude and introducing common mode levels

This annex describes a circuit that may be used for degrading the signal amplitude and introducing the common mode levels needed to execute the receiver and Cable Assembly tests. Jitter introduction is accomplished upstream of this circuit.

The terminators should not be varied to change input signals, since the terminators are normally inaccessible. Varying the terminators may introduce reflections. The suggested circuit maintains the 75 Ω environment while allowing the signal levels to be adjusted. Also, by adding noise to the external terminator power source one may vary the common mode levels at the receiver input.

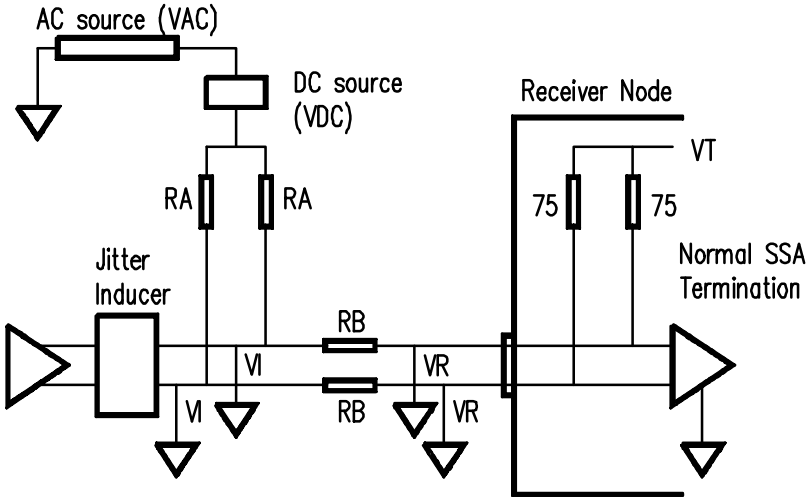


Figure G.1 - Signal degrader, common mode level generator, jitter inducer circuit

Figure G.1 shows the basic circuit and architecture. By keeping both RAs and both RBs the same for both lines, this circuit allows the impression of both a.c. and d.c. common mode levels. In addition by varying the values of RA and RB one may maintain the 75 Ω (single ended) environment at different attenuation levels.

In order to keep the 75 Ω environment the parallel combination of RA with RB+75 as seen from the driver should be 75 Ωs. This requires that RA(RB+75)/(RA+RB+75) = 75. This relationship between RA and RB should be maintained under all conditions. RA as a function of RB is therefore:

$RA = 75(RB+75)/RB$

RB as a function of RA is:

$RB = 75^2/(RA-75)$.

The voltage attenuation *A* is defined as the ratio of the voltage into the degrader circuit (VI) to the voltage at the receiver input (VR). This is a single ended calculation but directly translates to the differential attenuation as long as both RAs and both RBs are the same.

If the current through RA is I1 and the current through RB (and through the terminator) is I2 then the attenuation is given by:

$A = RA*I1/75*I2$

The ratio of I1 to I2 is simply the current division (RB+75)/RA.

This gives a simple relationship between A and RB:

$RB = 75(A-1)$

Invoking the 75 Ω requirement RA = 75*A*/(*A*-1).

The common mode noise levels may be adjusted by changing the amplitude of VAC in Figure G.1. These levels are reduced by the voltage division of RA, RB and RT. The general formula for the common mode levels at the receiver is:

VR = VAC*75/(RA+RB+75)

For a specific common mode level VAC is given by:

VAC = VR(RA+RB+75)/75.

For d.c. common mode levels these formulas also apply.

Annex H
(informative)
Preferred test configurations for SSA links

This annex defines recommended copper Cable Assembly lengths to be used when comparing different SSA implementations as shown in Table H.1. The lengths are determined by the speed of the link, whether internal or external, and by the dominant application feature of interest.

Table H.1 - Test configurations

Environment	20 MB/s length	40 MB/s length	Application Feature
Internal	0,05 m	0,05 m	Short distance between nodes
Internal	0,5 m	0,25 m	Resonance
Internal	3 m	3 m	Longest likely
External	0,5 m	0,25 m	Resonance
External	5 m	5 m	Common likely length
External	25 m	25 m	Longest likely

Annex I
(informative)
Implementation guidelines

I.1 Guidelines for printed circuit board design

The terms used in this clause are defined as follows:

a) Line path: The electrical conductor between the port connector and the termination circuitry, commonly the termination resistor (see Figure I.1).

b) Line + path: The line path for the + signal.

c) Line - path: The line path for the - signal.

d) Stub: Any electrical path connecting to the line path but not part of the line path (see Figure I.2).

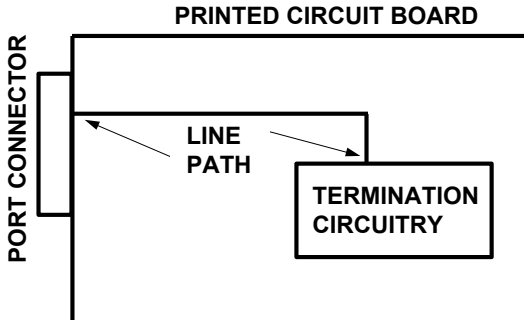


Figure I.1 - Line path definitions

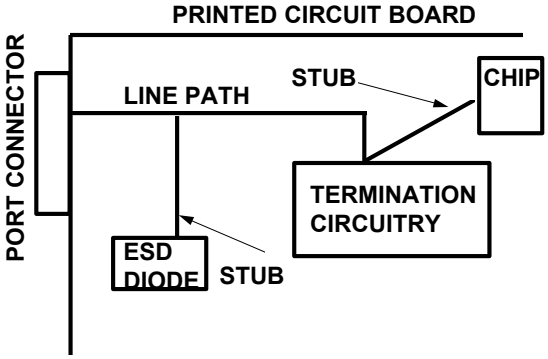


Figure I.2 - Stub examples

The following guidelines[2] should be followed when designing printed circuit boards using SSA.

a) Isolate other active signals from the line path on the printed circuit board.

b) Stubs should be minimized and not exceed 0,5 inch in length.

c) Capacitance to ground on stubs should be minimized.

[2]Refer to Montrose, Mark I.,Printed Circuit Board Design Techniques for EMC compliance, IEEE press 1996 (ISDN 0-7803-1131-0) for more details

d) Line + paths and line - paths should be laid out as 75 Ω single ended traces on one signal layer, preferably on top or bottom layers.

e) Isolate SSA ports from each other.

I.2 ESD protection for SSA ports

The designer of SSA devices for use within a chassis or system is minimally impacted by the possibility of electrostatic discharge causing damage to the device. This assertion is based on the fact that normal handling of these devices includes the use of body ground straps and related means of ESD protection. Designers of adapters, switches and other devices with external connectors may assume that ESD protection discipline is used during installation. Following installation, ESD protection cannot be assumed. Connectors used on external ports have their pins near the surface of the connector, so that in normal use, electrostatic discharge from a user s body should be anticipated to the pins and to the devices connected to the pins. In order to prevent destruction of the device, designers of devices and systems with external ports are advised to provide protection from ESD.

There are several standards that describe models of the human body for ESD. IEC 801-2 calls out a model of the human ESD characteristics consisting of a main (body) capacitance, a series resistor, and a secondary (hand) capacitance then connected to the test finger that is discharged to the device under test (DUT) as shown in Figure I.3. The total capacitance is 150 pF, with a 330 Ω series resistor.

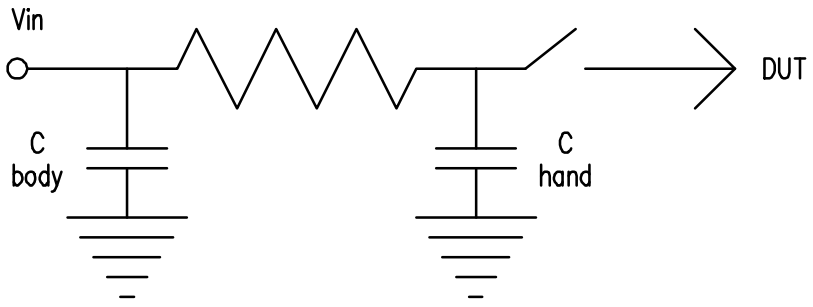


Figure I.3- Human ESD characteristics model

Either direct contact or air discharge may be used, with the initial voltage on the capacitors set according to the Table I.1 below. The current waveform has two peaks, the first, emulating the discharge of the hand capacitance, has a rise time of 1 ns and a duration of approximately 3 ns, superimposed on a slower waveform emulating the body capacitance discharge peaking at 30 ns. Table I.1 indicates the voltages depending on the level of the test. Level 1 is the least stringent, and is typical of the tolerance level offered by today s silicon implementations. The Generic ESD immunity standard EN50082-1 calls out the level 3 (8 kV air discharge) test for most equipment that is exposed to ESD.

Table I.1- ESD characteristics of the human model

Level	Direct Injection voltage	Air Discharge Voltage	First Current Peak (± 10%)	Current peak at 30 ns (± 30%)	Current at 60 ns (± 30%)
1	2 kV	2 kV	7,5 A	4 A	2 A
2	4 kV	4 kV	15 A	8 A	4 A
3	6 kV	8 kV	22,5 A	12 A	6 A
4	8 kV	15 kV	30 A	16 A	8 A

The standard describes tests applying 300 such pulses and keeping statistics on transient and soft recoverable, soft non-recoverable and hard errors. No operator intervention is required to recover from transient and soft-recoverable errors. The Link ERP of the link should handle all such errors. Soft non-recoverable errors require a node reset and re-start, and hard errors require equipment repair. The definition of a tolerable failure rate is subjective, but typical values should be no more than 0,5% hard errors, 5% soft non-correctable, 94,5% soft correctable and transient errors.

Annex J
(informative)
Reference for copper, polymer dielectric, non-equalized SSA cable assemblies

This Annex contains an example of a set of electrical parameters that have been found to work for relatively long copper cables with polypropylene dielectrics. The requirements in Table J.1 have been found satisfactory for shielded and unshielded copper, non-equalized, polymer dielectric SSA cable assemblies of several meters in length.

Table J.1 - Characteristics for non-equalized copper polymer-dielectric cables

Description	Value
Differential characteristic impedance of a Line (Measured with a differential TDR)	150 Ω ± 10%
Attenuation of a Line (Measured with a network analyzer)	<4,2 dB @ 200 MHz <7,8 dB @ 600 MHz
Skew between Line+ and Line- of the same Line (Measured with a 2 channel TDR)	<0,5 ns
Differential cross talk between Lines (near end with 1 ns rise time on driven differential pair)	<5%

All measurements are intended to apply to completed cable assemblies. All measurements except possibly cross talk are usually dominated by the cable media and therefore may avoid requiring the full Cable Assembly for execution.

The differential characteristic impedance should be measured in the following way:

a) the length of the cable sample should be appropriate for the instrumentation;

b) the signal pair being measured should be defined according to its identification and position in the cable layout and terminated with 150 Ω;

c) at the end where the TDR is attached all shields and conductors not directly part of the signal pair under test should be connected together and grounded and at the far end shall be left unconnected;

The cross talk should be measured in the following way:

a) the complete Cable Assembly with connectors and backshells (if used) should be used;

b) a differential voltage signal with a 1 V peak to peak amplitude and approximately a 1 ns rise/fall time should be supplied to the near end of the driven pair;

c) the driven pair should be terminated with a 150 Ω resistor at the far end;

d) the victim pair (the measured pair) should be terminated at both ends with a 150 Ω resistor (see Figure J.1).

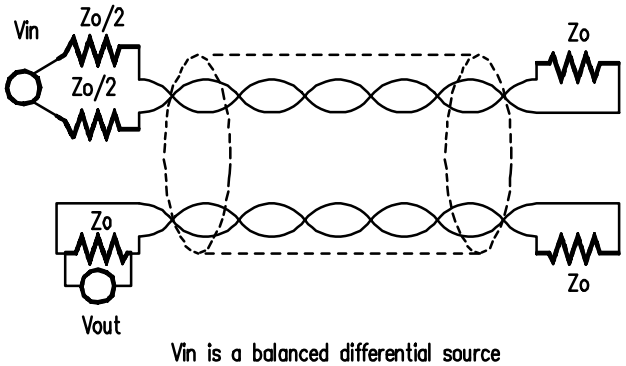


Figure J.1 - Cable Assembly cross talk measurement

Annex K
(informative)
The use of Fiber-optic Port Connection Couplers With SSA

This Annex is intended to expand upon the Normative sub-clause 7.5.5 defining Port Connection Couplers to clarify how Fiber-optic logic-light/light-logic links may be used in SSA.

Complex connections behave electrically as a cable behaves as measured at the input and output connectors. Fiber-optic links may be constructed to be used as the sole element in a complex connection between 2 ports, or may be built to be used as one element of a complex port connection.

If the link will be the sole element in a complex port connection, the input to the logic-light end of the link will be as described in the standard s line driver output definition. Building the logic to light converters into the connector or the use of a short cable to the converter would be expected implementations. The SSA input lines to the converter need to be properly terminated to minimize reflections and jitter. The output of the light-logic end of the link would need to be electrically no worse than that defined in the Line Receiver sub-clause 7.2 of the standard at the connector. This type of link could not be connected to an additional line segment such as a long cable, since the amplitude and jitter budget of the link was already consumed.

If the link is intended to be used with long cables, then the input to the logic-light end of the link would need to accept worst case Line Receiver signals as defined in section 7.2 of the standard. At the output of the light-logic end of the link, the signals would need to meet the jitter and amplitude requirements as defined in the Line Driver sub-clause 7.1 of the standard. This implies some sort of jitter reduction as well as amplification.

Within the optical section of the link, an implementer has few restrictions governing the selection of single vs. Multi-mode, fiber type, LED or Laser source, wavelength, launch power, etc. SSA does not limit the choice of characteristics, and leaves the compliance with other standards such as Laser Safety to the implementer.

The standard places 2 additional requirements on SSA complex port connections. The first is the ACK time-out. Two nodes not capable of extended distance operation have a 25 microsecond ACK time-out. Two nodes capable of extended distance operation have a 100 microsecond ACK time-out. If the complex port connection containing the fiber-optic link exceeds these limits round trip from port to port including the remote port s processing time, then the standard requirement will not be met. Since the speeds of processing will vary, some margin should be left in the total round trip propagation delay of the link, 1-2 microseconds being a reasonable amount. In most implementations, the generation of ACK is performed by dedicated hardware and will occur more quickly than this. Allowing 2 microseconds for margin means that the round trip propagation delay of the link should not exceed 23 microseconds for standard links and 98 microseconds for extended distance links.

The second requirement placed by the standard is that of error rate. Sub-clause 7.6 of the standard requires a full order of magnitude in the link bit error rate for purposes of accommodating noise that may be present during real system operation but not present during the execution of the tests defined in 7 (termed system noise). The receiver shall not exceed 10^{-13} bit error rate under the receiver tests but the individual links in the overall SSA system shall not exceed 10^{-12} bit error rate in operation.

The entire complex port connection defined in the standard has a bit error rate of 10^{-12} or better. A fiber-optic link should be designed and tested to meet this requirement in the intended complex port connection configuration.

Power for an external PCC is not guaranteed to be supplied by the SSA external connector. In sub-clauses 8.5.1.5 or 8.5.2.5, there is an optional 5 volt pin capable of supplying a minimum of 0.25 A. An implementation may use this power, but should provide an alternate method of obtaining any required power if the port connector does not provide it. SSA cables, as illustrated in the example in the standard , do not necessarily carry conductors for power. An implementation would need to provide additional conductors within a cable or as an additional cable to convey power from an SSA external connector or power supply to the optical converter.

Interrupting an optical path should cause the optical receiver to not generate transitions on LineIn, resulting in detection of either a Line Fault or No Characters Received.