Date: October 11, 2007
To: T10 Technical Committee
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Subject: SAS-2 Calibration of Jitter Measurement Devices

Abstract: This proposal defines a calibration procedure for jitter measurement devices to be added to Annex B of SAS-2, pending the approval of 07-339, SAS-2 6Gbps PHY Electrical Specification (that introduces the jitter transfer function (JTF) concept to the SAS electrical specification). This proposal includes additional background information regarding the operation of phase locked loop clock recovery. Originally posted as a document to the T10 reflector by Chuck Hill, Alvin Cox has edited the content into a proposal format convenient for inclusion in the SAS-2 specification.

Referenced section numbers based on 07-339r5.

Revision History:
r0: Initial posting.
r1: Editorial changes in PLL clock recovery section.

B.10 Calibration of Jitter Measurement Devices

The response of a jitter measurement device (JMD) to known jitter levels is calibrated and verified in two frequency bands. The lower frequency band is at the fundamental of the SSC (i.e., 30 kHz) and the second higher frequency band is in the transition region between the reference clock tracking and not tracking the jitter (i.e., approximately 2.6 MHz). The reference clock is part of the JMD and may be implemented in hardware or software. By calibrating the JMD to these two bands, the response to jitter is calibrated and allows for improved correlation among JMDs.

The lower frequency band requirement is tested with a D24.3 pattern on which 20.8 ns pk-pk sinusoidal phase (time) modulation at 30 kHz ±1% is added. The ratio of the reported jitter to the amount actually applied (measured independently) is the attenuation and shall meet the requirement specified in 5.3.5.1.

The specification defines two parameters related to SSC, f_{baud} (e.g., 6 GHz for 6 Gbps) and SSC_{tol} (e.g., the spread spectrum modulation deviation). The frequency deviation (of the clock in the data source) is related to the SSC frequency deviation by

$$\Delta f = SSC_{tol} f_{baud}$$

The sinusoidal phase modulation is related to frequency modulation by

$$\Delta f = f_m \ \Delta\phi$$

where Δf is the frequency deviation in Hz, f_m is the modulation frequency in Hz, and $\Delta\phi$ is the phase deviation in radians.

The phase deviation is related to the phase modulation in time by

$$\Delta\phi = 2\pi f_{baud} \Delta T$$

Since SSC profiles are the option of the implementer, a triangular SSC profile has been assumed. For calibration purposes, ΔT is the integral of a triangular, 5000 ppm, center-spread SSC profile at 30kHz which is equivalent to a sinusoidal phase (time) modulation with a peak-to-peak amplitude of 20.83 ns, independent of f_{baud}.

From these relationships, an expression for the SSC frequency deviation from the JTF test parameters is given, calculated for the test conditions and shown to be within the specification limits.

$$SSC_{tol} = 2\pi f_m \Delta T = 2\pi (3.0\text{x}10^{4})(20.83\text{x}10^{-9}) = 3926\text{ppm}$$

From these calculations, either frequency or phase modulation may be used. A separate means of verifying the level of the modulation is used to make sure the test conditions are correct. The independent, separate means of verification of the 30 kHz test signal is equivalent to a frequency demodulator or wide range, phase demodulator.

Two tests are performed in the upper frequency band. The adjustment of the -3 dB bandwidth of the JTF and the verification of the peaking (see 5.3.5.1). Both of these tests use a D24.3 pattern with sinusoidal periodic phase modulation, or periodic jitter (PJ) that has been independently verified to produce 0.3 UI ± 10% pk-pk consistently over a frequency range of 0.5 MHz to 50 MHz. In both tests a 0 dB reference level is initially determined so all other measurements are relative to this level, not the absolute level of the source. It is important that the PJ source level does not vary in amplitude over this test range, or the variation needs to be extracted in the final calculations.

For the tests in the upper frequency band it is necessary to have a phase or jitter modulator. The independent separate means of verification of the 2.6 MHz and 50 MHz test signals is equivalent to a deterministic jitter measurement with constant clock.

There are two typical JMD adjustments for clock recovery: loop bandwidth and “peaking”, “damping”, or ζ. These adjustments may refer to the closed loop response or be specific to a particular design, so they may not be used directly to ensure the JTF response to jitter. It is suggested that the loop bandwidth be adjusted initially (with the “peaking” fixed) and if both the low frequency band requirements and the high frequency band requirements cannot be simultaneously be met, the peaking be adjusted to modify the JTF shape in the upper band. In the case of hardware based reference clocks, moderate levels of “peaking” may be required to achieve the proper attenuation at 30 kHz. The peaking setting is usually specific to the JMD. With software based clock recovery, the suggested starting “peaking” level or “damping” may be low, close to the critically damped condition of $\zeta = 0.707$.

The test sequence for all measurements also removes the baseline deterministic jitter, DJ of the source and JMD such that what is being measured is the reported jitter only due to the added test jitter and not any baseline residual jitter in the test system. This is important to insure the accuracy of the measurement at low reported jitter levels.

JMD Calibration Procedure

This calibration procedure is based on the following performance requirements:

1) The -3 dB corner frequency of the JTF shall be 2.6 MHz +/- 0.5 MHz.
2) The magnitude peaking of the JTF shall be 3.5 dB maximum.
3) The attenuation at 30 KHz +/-1% shall be 72 dB to 75 dB.

The JTF -3dB corner frequency and the magnitude peaking requirements shall be measured with sinusoidal PJ applied, with a peak-to-peak amplitude of 0.3 UI +/-10%. The relative attenuation at 30 KHz shall be measured with sinusoidal phase (time) modulation applied, with a peak-to-peak amplitude of 20.8 ns +/-10%.

Resource requirements:

Pattern Generator for SAS signals

Sine wave source, 30 kHz, and 0.5 MHz to 50 MHz.
Test cables
Jitter Measurement Device

The response to jitter of the JMD (the reference clock is part of the JMD) is measured with three different jitter modulation frequencies corresponding to the three cases:

1. SSC (full tracking),
2. jitter (no tracking), and
3. the boundary between SSC and jitter.

The jitter source is independently verified by separate means. This ensures the jitter response of the JMD is reproducible across different test setups.

The three test signals are:

1. a 1.5 GHz ± 0.01% square wave (which is a 6Gbps D24.3, 00110011 pattern) with rise time longer than 0.25 UI 20% to 80% and with a sinusoidal phase modulation of 20.8 nS ± 10% peak to peak at 30 kHz ± 1%,
2. a 1.5 GHz square wave with a sinusoidal phase modulation of 100 pS ± 10% peak to peak at 50 MHz ± 1%, and
3. a 1.5 GHz square wave with no modulation.

An independent, separate means of verification of the test signals is used to make sure the level of the modulation is correct.

The test procedure checks two conditions: the JTF attenuation and the JTF bandwidth.

1. Adjust the pattern generator for a 6 Gbps D24.3 pattern (00110011b, with a rise time within specified limits) modulation to produce a 30 kHz ± 1%, 20.8 ns ± 10% pk-pk sinusoidal phase modulation.
2. Verify the level of modulation meets the requirements and record the pk-pk level, **DJSSC**. The independent, separate means of verification of the 30 kHz test signal is equivalent to a frequency demodulator or wide range phase demodulator. This may be measured with:
    a. a time interval error plot with constant frequency clock on a real time oscilloscope,
    b. an equivalent time oscilloscope, or
    c. a frequency demodulator.
3. Apply the test signal to the JMD. Turn off the sinusoidal phase modulation. Record the reported DJ, **DJSSCOFF**.
4. Turn on the sinusoidal phase modulation. Record the reported DJ, **DJSSCON**.
5. Calculate and record the level of measured DJ by subtracting the DJ with modulation off from DJ with modulation on, **DJMSSC = DJSSCON - DJSSCOFF**. Calculate the jitter attenuation by 20Log(**DJMSSC** / **DJSSC**). This value shall fall within the range of -72 dB to -75 dB. Adjust the JMD settings to match this requirement.
6. Adjust the pattern generator for a 6 Gbps D24.3 pattern (00110011) and modulation to produce a 50 MHz ±1%, 0.3 ± 10% UI pk-pk (100 pS) sinusoidal phase modulation, also known as periodic jitter, PJ.
7. Verify the level of modulation meets the requirements and record the pk-pk level, **DJM.** The independent verification of the 50 MHz test signal is a jitter measurement by separate means from the JMD under calibration. This may be measured with:
    a. a time interval error plot with constant frequency clock on a real time oscilloscope
    b. an equivalent time oscilloscope with histogram and constant frequency clock
    c. a bit error rate tester (BERT) using a constant frequency clock, or
    d. a spectral analysis with the Bessel expansion of angle modulated sidebands.
8. Apply the test signal to the JMD. Turn off the sinusoidal phase modulation. Record the reported DJ, **DJMOFF**.
9. Turn on the sinusoidal phase modulation. Record the reported DJ, **DJMON**.
10. Calculate the difference in reported DJ for these two cases, **DJMM = DJMON - DJMOFF** Calculate the -3dB value: **DJ3DB** = **DJMM** * 0.707

11. Adjust the frequency of the PJ source to 2.6 MHz ± 0.1 MHz. Measure the reported DJ difference between PJ on versus PJ off **DJ = DJON - DJOFF** and compare to the (DJ -3dB) value, **DJ3DB**. Shift the frequency of the PJ source until the reported DJ difference between PJ on versus PJ off is equal to (DJ -3 dB). The PJ frequency is the -3 dB BW of the JTF; record this value **F3DB**.
12. Adjust the JMD settings to bring the PJ -3dB corner frequency to 2.6 MHz ± 0.5 MHz. Repeat steps 4 through step 12 until both the jitter attenuation and -3 dB frequency are in the acceptable ranges.
13. Check the peaking of the JTF. Adjust the pattern generator for a 6 Gbps D24.3 pattern and modulation to produce sinusoidal phase modulation (PJ) at the -3 dB BW frequency found above, and 0.3 ± 10% UI pk-pk (100 pS). Increase the frequency of the modulation to find the maximum reported DJ. It is not necessary to increase beyond 20MHz. Measure the reported DJ difference between PJ on versus PJ off, **DJPK = DJPKON - DJPKOFF**. Record this DJ difference (**DJPK**) and frequency, **F3PK**.
14. Calculate the JTF Peaking value: 20Log (**DJPK** / **DJMM**). Record this value.

Background information (not part of standard)

In serial interfaces with embedded clocks, a clock is derived from the data stream at the receiver. When spread spectrum clocking (SSC) is applied to the embedded clock, the spread spectrum frequency modulation needs to be considered as part of the clock so that its resulting zero crossing shifts in the data pattern are not included in the jitter measurements.

Devices that recover the embedded clock for jitter measurement need to be verified for proper operation and calibrated if necessary. The verification process is done by measuring the response of the jitter measurement device (JMD) to known stimuli. The JMD is calibrated by adjusting it to provide the proper response for three conditions: the attenuation, bandwidth, and peaking.

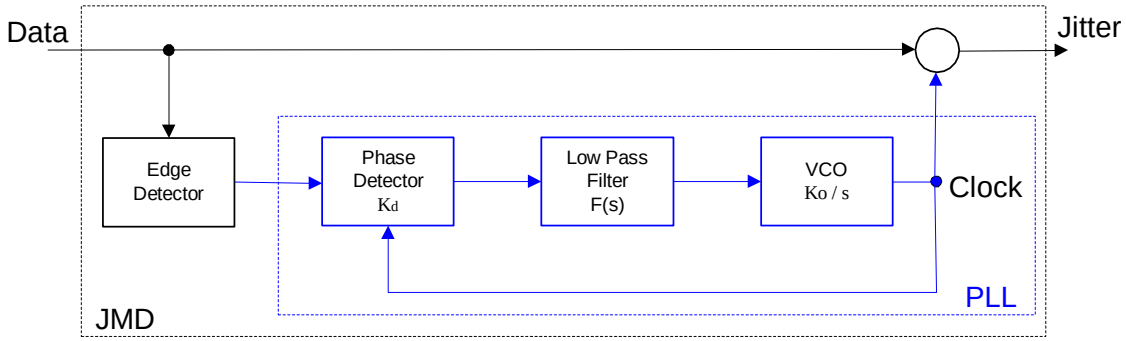
Phase Locked Loop Clock Recovery
A Phase Locked Loop (PLL) is a common way of achieving the clock recovery with an appropriate jitter rejection and SSC tracking. To achieve this separation, at least two poles at or near the origin are necessary. Such a PLL is called second order. A PLL is a feedback control device with an open loop gain, and a closed loop gain. A second order type 2 PLL has an open loop gain with two poles at the origin and a compensating zero for stability. The open loop gain of any PLL is

$$G(s) = \frac{K_o K_d F(s)}{s}$$

The closed loop gain is a function of the open loop gain.

$$H(s) = \frac{G(s)}{1 + G(s)}$$

In many Jitter Measurement Devices (JMD's) the reference clock is not observable. Since the closed loop response cannot be measured, the JMD cannot be verified against the verification requirements. However, JMD's measure jitter, and that is observable.



In response to jitter, the jitter transfer function is $J(s) = 1 - H(s)$

A second order type 2 PLL has loop filter gain of $F(s) = K_f \dfrac{s + \omega_z}{s}$

Define the DC loop gain as $K = K_o K_d F(0)$

From this the second order type 2 PLL closed loop response is represented by the equation below. It shows two parameters to set to achieve a 3dB point, the loop gain and the zero position.

$$H(s) = \frac{K}{\omega_z} \frac{\left(s + \omega_z\right)}{s^2 + \dfrac{K}{\omega_z} s + K} = K \frac{\left(1 + \dfrac{s}{\omega_z}\right)}{s^2 + \dfrac{K}{\omega_z} s + K}$$

The closed loop response expressed as a 2nd order system (servo terminology) is

$$H(s) = \frac{{\omega_n}^2 \left(1 + \dfrac{s}{\omega_z}\right)}{s^2 + 2\zeta\omega_n + {\omega_n}^2}$$

where the natural frequency is

$$\omega_n = \sqrt{K} = 2\omega_z\zeta$$

and the damping ratio is

$$\zeta = \frac{\sqrt{K}}{2\omega_z} = \frac{\omega_n}{2\omega_z}$$

The jitter response is, showing two parameters to set to achieve a 3dB point, the loop gain and the zero position:

$$J(s) = 1 - H(s) = \frac{\left(s + 2\zeta\omega_n - {\omega_n}^2\right)s}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} = \frac{s^2}{s^2 + \frac{K}{\omega_z}s + K}$$

The bandwidth of the closed loop response is the solution to

$$20\log\left(\left|H(s)\right|\right) = 20\log\left(\left|K\frac{\left(1+\frac{s}{\omega_z}\right)}{s^2 + \frac{K}{\omega_z}s + K}\right|\right) = 3$$

The jitter transfer magnitude response is

$$20\log\left(\left|J(s)\right|\right) = 20\log\left(\left|1 - H(s)\right|\right) = 20\log\left(\left|\frac{s^2}{s^2 + \frac{K}{\omega_z}s + K}\right|\right)$$

The closed loop response (verification requirement) and the jitter transfer (experimentally observable) are set by the loop gain, the zero position, and the definition of a type 2 PLL. To achieve a reproducible jitter transfer function, the important parameters to control are the loop gain and the zero position.

The test procedure sets the loop gain and zero position to achieve a consistent response to jitter and SSC in the test setup. Proper operation of the test setup is verified by observing its response to jitter.

Data Transition Density

The response of the PLL changes with the number of data transitions that occur within a given period of time. The number of data transitions that occur within a given period of time is called the data transition density. The phase detector provides a phase (time) difference each time a data transition occurs. When more data transitions occur, more corrections result. As a result, the phase detector gain K_d changes proportionally with data transition density, as does the loop gain K. In the type 2 PLL, the loop gain is falling at 20dB/decade at unity gain crossover and in the region where the jitter transfer 3dB point occurs. Therefore, the jitter transfer 3dB point varies proportionally with data transition density.

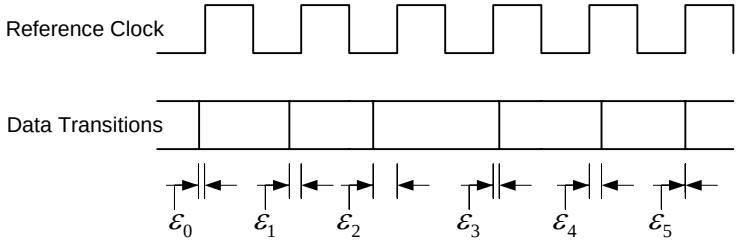
The bandwidth variation of a PLL may be examined through an analysis of the PLL as an estimator of time (phase). To do this, a description of jitter is required. Consider the times when the clock edges occur. A perfect clock has edges that occur at multiples of a given period, T, and each clock edge is identified by an integer index. The time of ideal clock edges is expressed by

$$t_C(i) = i\,T$$

Data transitions occur on clock edges. Ideal data transitions occur at the same time as clock edges. In real systems, the data transitions do not occur at ideal times. The time error from ideal of the data transitions is called jitter and is expressed by

$$t_D(i) = i\,T + \varepsilon_i$$

where the ε_i is the time deviation from ideal, or the clock to edge jitter. This is illustrated below.



The response time of the PLL is in the microseconds because the bandwidth is in the megahertz. Over this time interval, thousands of bit transitions occur; hence the loop converges to a long term average. Over a time interval of tens of bits, the action of the PLL on the time deviations or error ε_k tends to simply average the error.

For a 01010101b signal with five bits and errors at each data edge, the PLL correction is

$$\sum_{i=0}^{4} \frac{\varepsilon_i}{5} = \Delta t$$

For a signal with a run length of five, there are only two data transitions and the phase detector gain and PLL bandwidth are lower. The error is still averaged with a lower scaling factor since not as many edges are present.

$$\frac{\varepsilon_0 + \varepsilon_4}{5} = \Delta t$$

Suppose it was desired for the bandwidth to be constant over data transition density. In a practical phase detector, this requires the error in the fifth bit be amplified. The error in the first bit is not amplified since the PLL is causal.

$$\frac{\varepsilon_0 + 4\varepsilon_4}{5} = \Delta t$$

Each timing error ε_k no more indicates the true data transition time than any other timing error, therefore the error in Δt would be greater since the error term ε_4 is weighted too heavily. It is best for the errors to be weighted equally. Hence, the PLL as an estimator of time (phase) is better when the PLL bandwidth changes with data transition density.